Bulletin CA-176

A Texas Instruments Application Report

Series 54S/74S Schottky TTL Applications

TABLE OF CONTENTS

Section	*Title*	*Page*
1.0	INTRODUCTION TO SCHOTTKY CLAMPED TTL	1
1.1	Speed-Power Slots Filled By Schottky TTL	1
1.2	Additional Advantages Offered By Schottky TTL	2
1.3	Concepts of Defining Series 54S/74S Schottky Functions	3
1.3.1	Compatibility With Other TTL	3
1.3.2	Fan-Out	3
1.3.3	Pinouts	3
1.4	Utilizing the SBD	3
1.4.1	Analysis of Schottky-Clamped Transistor	3
1.4.2	Analysis of Series 54S/74S NAND Gate	4
1.4.3	Analysis of Clocking – Series 54S/74S Flip-Flop	6
1.5	Circuit Parameters	6
1.5.1	Transfer Characteristics	7
1.5.2	Input Characteristics	9
1.5.2.1	Low-Level Input Current	9
1.5.2.2	Input Clamping Diode Tests	9
1.5.2.3	High-Level Input Current	9
1.5.2.4	Input Breakdown Tests	10
1.5.2.5	Equivalent A-C Impedance of Inputs	10
1.5.2.6	A-C Noise Immunity	11
1.5.2.7	Schmitt-Trigger Input Thresholds	11
1.5.3	Output Characteristics	12
1.5.3.1	High-Level Output Characteristics	12
1.5.3.2	Low-Level Output Characteristics	13
1.5.4	Switching Speed	13
1.5.5	Supply Current Characteristics	16
1.5.6	D-C Noise Margins	17
1.5.7	Noise Rejection	17
2.0	GUIDELINES FOR SERIES 54S/74S SCHOTTKY TTL SYSTEM DESIGN	19
2.1	Power Supply Regulation	19
2.2	Power Supply Ripple	19
2.3	Noise Considerations	19
2.3.1	Noise Types and Control Methods	23
2.3.2	Shielding	23
2.3.3	Grounding and Decoupling	23
2.3.4	Cross Talk	27
2.3.4.1	Back-Panel Interconnections	27
2.3.4.2	Printed Circuit Card Conductors	29
2.3.5	Transmission-Line Driving Reflections	31

APPENDICES

A.	NORMALIZED LOAD FACTORS	36
B.	SERIES 54S/74S PIN ASSIGNMENT DIAGRAMS (applicable for all package types)	38
C.	LETTER SYMBOLS, TERMS, AND DEFINITIONS	43

LIST OF ILLUSTRATIONS

Figure	*Title*	*Page*
1.1	Speed-Power Spectrum of Series 54/74 TTL Family	2
1.2	Series 54/74 TTL Family Compatible Logic Levels Showing D-C Noise Margins	3
1.3	Fan-Out Capability versus Series 54/74 Loads	3
1.4	The Baker Clamp	4
1.5	The Schottky-Clamped Transistor	4
1.6	The Schottky-Barrier Diode	4
1.7	Schottky-Barrier Diode Energy Diagrams	5
1.8	Metal-N Diode I-V Characteristics	5
1.9	Differences Between the PN and Schottky-Barrier Diodes	5
1.10	The STTL NAND Gate Schematic	6
1.11	Timing Relationship of Flip-Flop to Clocking Transition	7
1.12	SN54S/74S112 Flip-Flop Schematic Diagram	7
1.13	Voltage Transfer Characteristics of Typical TTL/STTL NAND Gate	8
1.14	V_O and V_T versus Temperature	8
1.15	I_I versus V_I	9
1.16	Equivalent D-C Circuit for STTL Input	9
1.17	Input-Clamping Diode Forward Voltage versus Temperature	10
1.18	High-Level Input Current versus Temperature	10
1.19	Equivalent A-C Circuit and Input Waveform	11
1.20	Noise Pulse Width versus Pulse Amplitude for STTL Gate	11
1.21	Transfer Characteristic of SN54S/74S132	11
1.22	Response of Standard Gate and Schmitt Trigger to Noisy Input	12
1.23	Series 54S/74S V_{OH} versus I_{OH} and Equivalent Schematic	13
1.24	Series 54S/74S V_{OL} versus I_{OL} and Equivalent Schematic	13
1.25	A-C Load Circuits and Voltage Waveforms	14
1.26	Switching Times versus Free-Air Temperature	15
1.27	Switching Times versus Supply Voltage	16
1.28	Typical Power Dissipation/Gate versus Frequency	17
1.29	Stray Coupling Capacitance	17
1.30	Evaluations of Gate Response to Ramp/Amplitude of Input	18
2.1	Effect of D-C Ground Levels on Apparent Input Levels	22
2.2	Effect of D-C Ground Noise on Noise Margin	22
2.3	Effect of Input Impedance on Input Noise	22
2.4	Low-Frequency Ripple Effects	22
2.5	Typical Logic Circuit with Noisy Inputs	23
2.6	Simplified Circuit of a Gate Driving a Loaded Transmission Line	23
2.7	Noise Generation Due to Poor Transmission Line Returns	24
2.8	Ideal Transmission-Line Current Handling	24
2.9	STTL Totem-Pole Output Stage	24
2.10	Circuit Showing Effective Capacitive Loading	25
2.11	I_{CC} Transient, Comparing TTL Types	26
2.12	Transmission-Line Power Buses	26
2.13	Capacitive Storage V_{CC} System	26
2.14	Commonly Used Power Distribution and Decoupling System	27
2.15	Equivalent Circuit for Sending Line	27
2.16	Coupling Impedances Involved in Cross Talk	28
2.17	Capacitive Cross Talk Between Two Signal Lines	28
2.18	Equivalent Circuit for Cross Talk	28
2.19	Microstrip Line	29

LIST OF ILLUSTRATIONS (Continued)

Figure	*Title*	*Page*
2.20	Strip Line	30
2.21	Line Spacing versus Cross Talk Constant	30
2.22	Cross Talk Test Circuit	30
2.23	Dimensional Data for Cross Talk Test Circuit	31
2.24	Voltage Waveforms of 16-Inch Conductor on Two-Sided Board	31
2.25	Series 54S/74S Bergeron Diagram	31
2.26	Series 54S/74S Driving Twisted Pair	31
2.27	Negative Transition – 100-Ohm Unterminated Line	32
2.28	Positive Transition – 100-Ohm Unterminated Line	33
2.29	Negative Transition – 50-Ohm Unterminated Line	33
2.30	Positive Transition – 50-Ohm Unterminated Line	34
2.31	Negative Transition – 100-Ohm Unterminated Line	34
2.32	Positive Transition – 100-Ohm Unterminated Line	34
2.33	Negative Transition – 50-Ohm Unterminated Line	35
2.34	Positive Transition – 50-Ohm Unterminated Line	35
2.35	Unterminated Line Driving/Receiving at 125 MHz	35

LIST OF TABLES

Table	*Title*	*Page*
1.1	Typical Performance Characteristics by TTL Series	2
1.2	Typical Output and Threshold Voltages for SN54S00/74S00 Gates	8
1.3	D-C High-Level Output Impedance of STTL Totem-Pole	12
2.1	Guidelines for System Design Using Series 54S/74S TTL	20
2.2	Typical Impedance of Microstrip Lines	30
2.3	Typical Impedance of Strip Lines	30

SERIES 54S/74S SCHOTTKY TTL APPLICATIONS

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PREFACE

This report is intended to assist the designers of high-performance digital logic systems with the utilization of Series 54S/74S Schottky-clamped* TTL circuits.

This report provides an expanded insight into the characteristics of Series 54S/74S Schottky-clamped circuits and also tabulates a set of guidelines which can be used as a basis for establishing system design rules.

After an analysis of the Schottky clamping techniques and circuits, Section 1 continues with an in-depth review of Series 54S/74S performance compared to the familiar Series 54/74 equivalent. Some subjects covered are:

- Transfer characteristics
- Input and output parameters
- Switching times
- Supply currents
- A-C noise immunity
- D-C noise margins

Section 2 is devoted to:

- Power supply considerations
- Noise sources and their abatement
- Back panel and printed circuit card wiring guidelines
- Line driving and receiving

A design guideline summary, Table 2.1, is included to provide the designer with a handy reference for the general rules concerning use of Series 54S/74S Schottky-clamped TTL.

Appendix A provides normalized loading/driving capability information. This can prove useful for designers mixing the various speed-power products available in all branches of the Series 54/74 TTL families. Appendix B provides pinouts of the Series 54S/74S devices.

As an extension of the TI TTL families, Series 54S/74S features complete compatibility with existing Series 54/74 families. In addition, pin-compatible functions of the most popular Series 54/74 functions, including MSI, are offered so that system upgrading can be as simple as merely substituting a Series 54S/74S version for Series 54/74 parts in speed-critical paths.

* Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

1.0 INTRODUCTION TO SCHOTTKY CLAMPED TTL

Series 54/74 transistor-transistor logic has, since its introduction in 1965, become the most popular digital integrated circuit logic family ever offered and is probably the easiest to use medium-to-high performance logic circuits available. Its popularity, coupled with high-volume production techniques, has vaulted TTL into a position where it is the most economical approach to the implementation of major portions of medium-to-high performance digital logic systems, from those making simple decisions to highly complex real-time computer installations handling world-wide data processing.

The economic demands to constantly improve the efficiency of these systems are evident, and Series 54/74 is expanding rapidly to include the broadest selection of medium-scale integrated (MSI) and large-scale integrated (LSI) circuits of any logic family. In addition, the technology was, and still is, pursued vigorously to ensure that the TTL system designer has the needed performance at his disposal. The performance advantages gained by Schottky-clamping the TTL circuit were considered and the announcement of Schottky (Series 54S/74S) catalog parts was made early in 1970.

1.1 Speed-Power Slots Filled By Schottky TTL

Digital integrated circuits have historically been characterized for both speed and power. In other words, Series 54/74 contains 10 nanosecond NAND gates and 35 megahertz flip-flops and Series 54L/74L contains 1 milliwatt NAND gates and 5 megahertz flip-flops. Obviously, either of these logic families could be used to design a 2-megahertz system, indicating that categorization strictly by speed or power is inconclusive with respect to system efficiency.

This situation is responsible for the use of the speed-power product efficiency index for digital circuits. It is a rating obtained by multiplying the speed in nanoseconds by the gate power dissipation in milliwatts, and can be used as an overall measure of the circuit's efficiency and performance.

Table 1.1 ranks the TI TTL Series by gate propagation delay times. In addition, the flip-flop clock frequency is listed for each family as an indicator for system performance.

Basically, the broad spectrum of the picojoule rating system is divided between circuits optimized for speed and those optimized for low power. Note in Table 1.1 that the Schottky-clamped circuits in each category represent a considerable improvement over the other TTL Series in both categories. The graphic analysis shown in Figure 1.1 includes representative data for the speed-power ranges experienced with the use of MSI. Further performance improvement with MSI is achieved since a large portion of the logic is internal to the chip and voltage swings can be reduced.

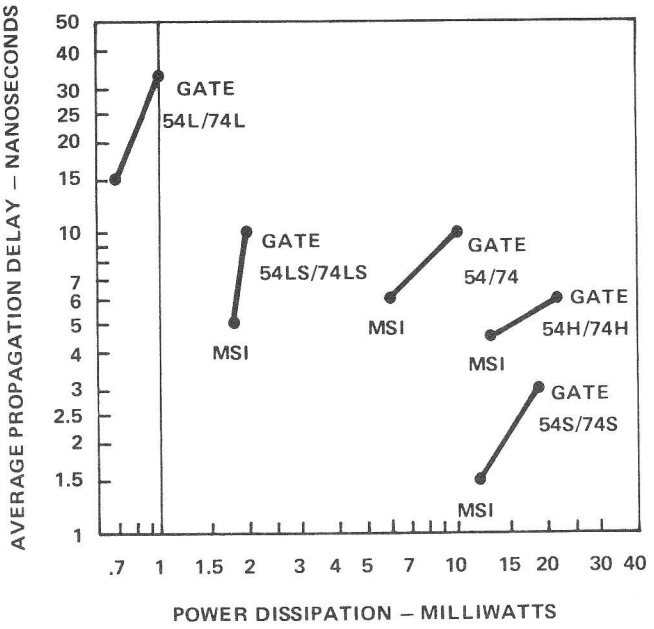


FIGURE 1.1 Speed-Power Spectrum of Series 54/74 TTL Family

1.2 Additional Advantages Offered By Schottky TTL

In addition to improved performance and efficiency, Schottky TTL permits:

a) Full compatibility with existing Series 54/74, 54H/74H, and 54L/74L. See paragraph 1.3.1.

b) Highest speed TTL ICs available with typical Series 54S/74S flip-flop toggle rates of up to 125 megahertz.

c) Guaranteed d-c parameters across the full operating ambient temperature range including 300 millivolts and at least 500 millivolts low-and-high logic d-c noise margins respectively.

d) Relatively stable switching times over the temperature range.

e) Selective upgrading of system performance due to pin compatibility.

f) Simplification of system design due to:
- Lower output impedances drive higher capacitance loads and further reduce susceptibility to a-c noise.
- Schottky-clamped input diodes suppress the effects of possible line ringing as undershoot is significantly reduced.
- Terminated lines or controlled-impedance circuit boards are not normally required.

g) Choice of 100 functions including high complexity MSI:

	SSI	MSI	TOTAL
Series 54LS/74LS	33	25	58
Series 54S/74S	24	18	42
TOTALS	57	43	100

Table 1.1 – Typical Performance Characteristics by TTL Series

Circuit Technology	Series	Gates			Flip-Flops
		Propagation Delay Time	Power Dissipation	Clock Input Speed-Power Product	Frequency Range
Schottky-Clamped	54S/74S	3 ns	19 mW	57 pJ	dc to 125 MHz
	54LS/74LS	9.5 ns	2 mW	19 pJ	dc to 45 MHz
Gold-Doped	54H/74H	6 ns	22 mW	132 pJ	dc to 50 MHz
	54/74	10 ns	10 mW	100 pJ	dc to 35 MHz
	54L/74L	33 ns	1 mW	33 pJ	dc to 3 MHz

1.3 Concepts of Defining Series 54S/74S Schottky Functions

The initial Schottky-clamped TTL circuits from TI were the 'S00 and 'S20 NAND gates and a basic dual flip-flop circuit. From its inception, Series 54S/74S was and is intended to supplement the basic Series 54/74 devices; therefore, complete functional compatibility and standardized pinouts are used. To further simplify use of this new family, assignments of corner locations for V_{CC}/ground connections are used.

1.3.1 COMPATIBILITY WITH OTHER TTL

In order to ensure complete electrical compatibility in systems using or intending to use mixtures of standard, low-power, high-speed, and Schottky devices, specific guidelines have been implemented which will not only ensure the continuation of the desirable characteristics of existing TTL but also incorporate newer techniques to improve performance and/or simplify the use of TTL. Figure 1.2 illustrates the essential comparative parameters of each family and shows that complete compatibility is maintained throughout the Series 54/74 family.

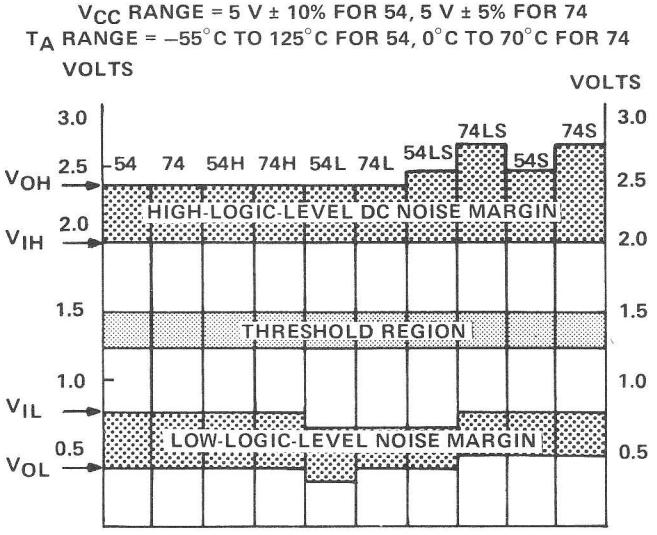


FIGURE 1.2 Series 54/74 TTL Family Compatible Logic Levels Showing D-C Noise Margins

1.3.2 FAN-OUT

The freedom to choose and implement logic using any of five performance ranges selectively in a single system is further simplified by compatible ratings for fan-out. Any of the TI TTL Series can be used to drive any other TI TTL Series without interface or level shifter circuits. This is illustrated graphically in Figure 1.3.

In addition, the concept of a double-ended circuit as the standard TTL output results in a low-impedance drive

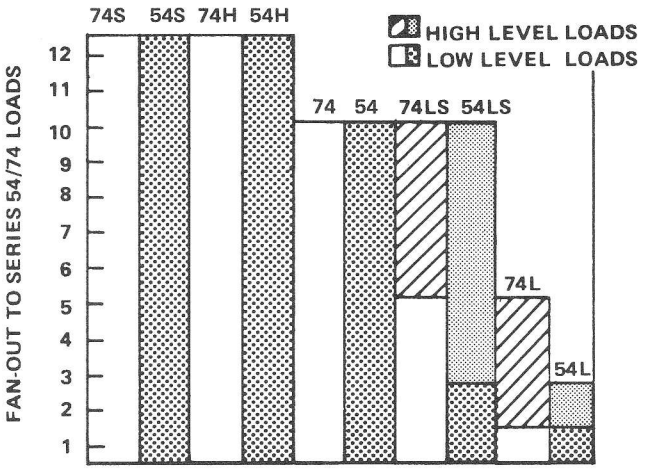


FIGURE 1.3 Fan-Out Capability versus Series 54/74 Loads

capability for sourcing or sinking current. It is easily adaptable for driving most MOS and CMOS circuits. Also, see paragraph 1.5.3 and Appendix A.

1.3.3 PINOUTS

Pin assignments for Schottky TTL circuits are the same as that of the corresponding Series 54/74 device. This means that all Schottky circuits in the dual-in-line packages are pin-for-pin with their corresponding Series 54/74 type.

Since 1969, all new TI TTL functions have been announced with standard (the same) pin assignments in both DIP and flat packages. Identical Schottky functions are offered with the same pin assignments in the three catalog packages (J C-DIP, N plastic DIP, W flat package). See Appendix B.

1.4 Utilizing the SBD

The Schottky-Barrier Diode Integrated Circuit Transistor is the result of two older concepts — The Baker clamp and the Schottky-Barrier-Diode (SBD) effect — applied in a relatively new technique to ICs. The result: transistor saturation is avoided and storage-related delay times are significantly reduced.

1.4.1 ANALYSIS OF SCHOTTKY-CLAMPED TRANSISTOR

A well-known way to avoid saturating a discrete transistor is to employ a Baker clamp. See Figure 1.4. The diode forward voltage is 0.3 volt to 0.4 volt as opposed to 0.7 volt for the base-emitter junction diode. When the transistor is turned on, base current will drive the transistor toward saturation. The collector voltage drops and the germanium diode begins conducting forward current, diverting excess base drive from the base-collector junction of the transistor. The transistor is held out of deep saturation, excess base charge is not stored, and turn-off time is dramatically reduced.

Obviously, a germanium diode cannot be incorporated into a monolithic silicon IC structure. The solution:

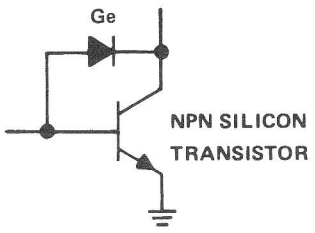
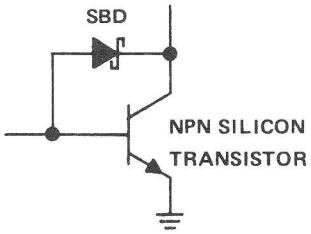


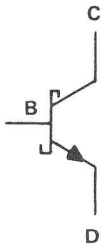
FIGURE 1.4 The Baker Clamp

replace the germanium diode with a silicon diode which has a lower forward voltage drop than the base-collector junction of the transistor. A normal PN diode will not meet this requirement. An ideal diode to implement this goal is the SBD. See Figure 1.5.

The SBD is a rectifying metal-semiconductor contact, formed between a metal and a lightly doped N semiconductor as illustrated in Figure 1.6.

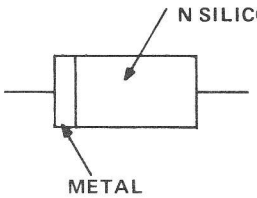


a) MONOLITHIC COMPOSITION



b) SYMBOL FOR MONOLITHIC SBD-CLAMPED TRANSISTOR

FIGURE 1.5 The Schottky-Clamped Transistor



a) COMPOSITION

b) SYMBOL

FIGURE 1.6 The Schottky-Barrier Diode

Figure 1.7 explains qualitatively the physics of an SBD. In a metal, only a fraction of the electrons (those outside the valence band) exist as free electrons. In a semiconductor, a store of free electrons exists near the bottom of the conduction band, created by adding donor impurity atoms. Under zero bias, the number of electrons crossing the barrier from both sides is the same, i.e., no net current flow.

Under forward bias (metal positive), there are many electrons with enough thermal energy to cross the barrier potential into the metal; this is called "hot injection." Because the barrier width is decreased as forward bias (V_F) increases, forward current will increase rapidly with increasing V_F.

When the SBD is reverse biased, electrons in the semiconductor require a much greater energy in order to be "boosted" over the barrier. However, electrons in the metal see a barrier potential from that side essentially independent of the bias voltage, and therefore a small net reverse current flows. Since this current flow is relatively independent of the applied reverse bias, the reverse current flow will not increase significantly until avalanche breakdown occurs.

The above explanation of the rectifying I-V characteristic of an SBD [Figure 1.5(a)] brings up one question: Since a collector contact is simply a metal-N semiconductor interface, why is the latter an ohmic contact while the SBD is a rectifying contact? The difference is controlled by the level of doping in the semiconductor material. See Figure 1.8. As the doping is increased, the contact becomes more ohmic.

Current in an SBD is carried by majority carriers and in PN junctions, current flow is determined by minority carriers. (See Figure 1.9.) The resultant minority carrier storage limits the switching time of a PN junction when switched from forward bias to reverse bias. A PN junction is inherently slower than an SBD, even when gold-doped.

Another major difference is the forward voltage drop. See Figure 1.9. For diodes of the same surface area, the SBD, regardless of the type of metal used, will have a larger forward current at the same forward bias. In other words, the SBD forward voltage drop is lower at a given current than a PN junction.

The SBD meets the requirements of a silicon diode which will clamp a silicon NPN transistor out of saturation.

1.4.2 ANALYSIS OF SERIES 54S/74S NAND GATE

The Series 54S/74S NAND gate, Figure 1.10, combines the desirable features of an improved TTL circuit with the technological advantages of full Schottky clamping to achieve very fast switching times at a reduced speed-power product. Specifically, some improvements and advantages are:

a) Full Schottky clamping of all saturating transistors virtually eliminates storing excessive base charge which significantly enhances turn-off time of the transistors. This is discussed further in paragraph 1.5.4.

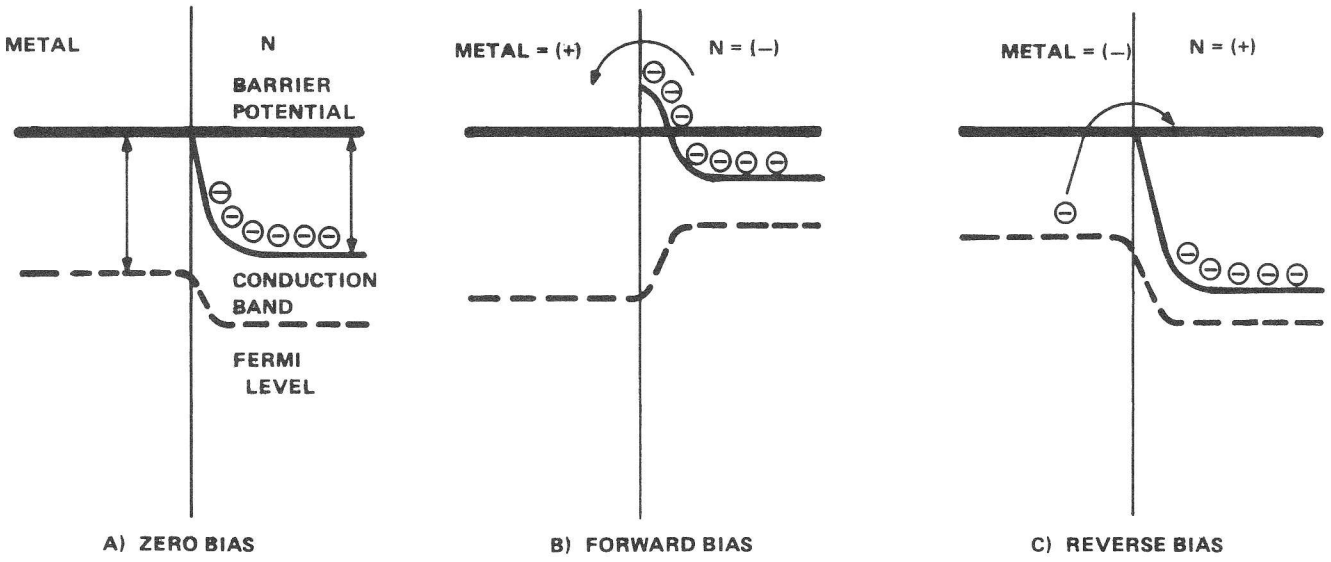


FIGURE 1.7 Schottky-Barrier Diode Energy Diagrams

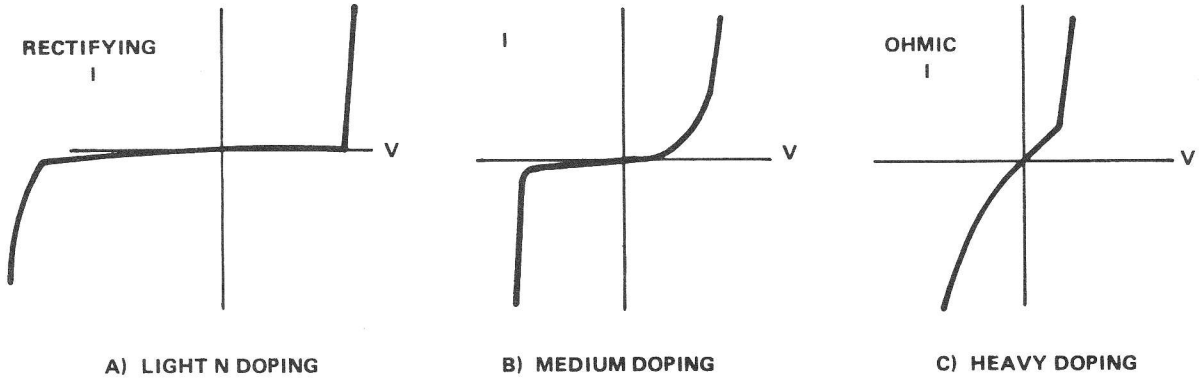


FIGURE 1.8 Metal-N Diode I-V Characteristics

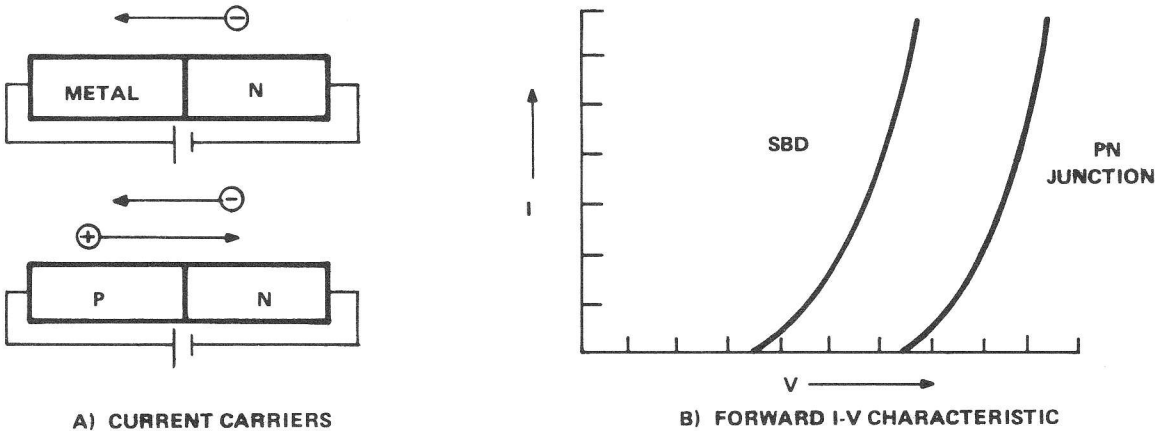
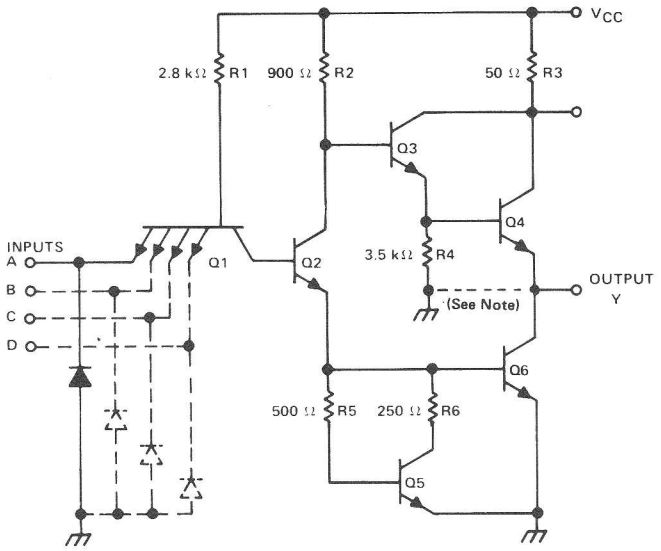


FIGURE 1.9 Differences Between the PN and Schottky-Barrier Diodes

b) Elimination of transistor storage time also provides stable switching times across the temperature range. Also discussed in paragraph 1.5.4.

c) An active turn-off is added to square up the transfer characteristic and provide an improved dynamic high-logic-level noise immunity. This is covered in detail in paragraph 1.5.1.



NOTE: Dotted line is alternate connection, and when used, R4 is considerably lower in value.

FIGURE 1.10 The STTL NAND Gate Schematic

d) Input clamping is implemented with Schottky diodes to reduce negative-going excursions on the inputs. Because of its lower forward voltage drop and fast recovery time, the Schottky input diode provides improved clamping action over a conventional PN junction diode. Also, see paragraph 1.5.2.

The input switching threshold (V_T) is set by transistors Q1, Q2, and Q6 with the following relationship:

$$V_T = (V_{BEQ2} + V_{BEQ6}) - V_{offset\ Q1}$$

This is identical to the method used in standard Series 54/74 TTL. The construction of the Schottky-clamped input transistor Q1 is such that the offset is virtually identical at its operating current levels with the nonclamped input of Series 54/74. The result is that V_T is within 100 millivolts of each other at about 1.3 volts for both Series 54S/74S and Series 54/74.

The Darlington output transistors Q3 and Q4, when on, establish the high-logic-level output voltage V_{OH} and supply the high-logic-level drive current, I_{OH}. From 0 to approximately −6 milliamperes, the effective output resistance is about 10 ohms. After saturation, the resistance is near 58 ohms and remains constant, primarily as a result of the 50-ohm collector resistor R3, through $V_O = 0$ volts (output shorted). The collector resistor R3 affords the short-circuit protection; however, duration of short-circuit as specified on the data sheet should be observed. This is designated as a maximum of one second and when no more than one output is shorted at a time.

The output configuration of some devices utilizes resistor R4 connected to the output (dotted line Figure 1.10) instead of to ground.

When not saturated, V_{OH} for either circuit is:

$$V_{OH} \approx V_{CC} - 2\,V_{BE}$$

which at $V_{CC} = 5$ V is about 3.4 V at $I_{OH} = -1$ mA.

The low-logic-level output voltage (V_{OL}) is established by transistor Q6 when it is on. This high-current transistor is driven in the on-state by a current path through R2 and Q2 when all inputs are high. Typically, sufficient base drive is supplied to keep Q6 fully on at an apparent resistance of ≈ 14 ohms while sinking up to 80 milliamperes of current at V_{CC} = 5 volts and T_A = 25°C, and the standard fan-out outputs (fan-out = 10) are guaranteed to sink 20 milliamperes of current across the operating V_{CC} and temperature ranges.

The active pull-down transistor, Q5, is instrumental in providing two very desirable improvements to the TTL circuit. When turned on, it removes base drive and causes Q6 to turn off more rapidly than a passive turn-off. At the same time, the reduced time of the transfer also reduces the duration of output overlap and the resultant current spike. See paragraph 2.3.3. In addition, the active turn-off circuit produces a square transfer characteristic.

1.4.3 ANALYSIS OF CLOCKING – SERIES 54S/74S FLIP-FLOP

Logic-level changes at the complementary outputs are virtually symmetrical. Instrumental in achieving this characteristic is the use of low-capacitance internal transfer nodes which react almost directly to the high-to-low transition of the clock input, Figure 1.11. The voltage at these nodes, A and B of Figure 1.12, is dependent upon the state of transistors Q6, Q7, Q18, and Q19. These voltage levels supply base-drive to the output transistors (Q10/Q11, Q12, Q22/Q23, and Q24) such that when the clock input is at a high-logic level and node A is high, Q20 is off and Q19 is on, and output $\overline{Q}$ is low (Q24 on and Q22/Q23 are off). This is a stable state regardless of the levels applied at the J and K inputs as Q7 is turned off by feedback from $\overline{Q}$, and Q6 is off because Q4 is on to remove the base drive from Q5.

To ensure that the bistable will change states on the high-to-low transition at the clock input, we must assume that the K input is high. Under this condition, Q3 will be off, Q15 will be on, and the clock input going low will turn on Q20 removing base drive from Q19. As Q15 is on, Q17 ensures that Q18 remains off and node B starts charging up to ≈ V_{CC}. This causes Q4 to turn off and enable base drive to Q6 which turns on. This causes Q12 to turn on and Q10/Q11 to turn off.

The timing relationship between the level changes at node A and the outputs are shown with respect to the clock transition in Figure 1.11.

1.5 Circuit Parameters[5]

Worst-case testing provides a built-in margin of safety. All d-c limits shown on the data sheet are guaranteed over the entire temperature range (−55 to +125°C for Series 54S and 0 to 70°C for Series 74S) and the entire supply voltage range (4.5 to 5.5 volts for Series 54S and 4.75 to 5.25 volts for Series 74S).

The following paragraphs describe the terminal characteristics for a typical Series 54S/74S TTL gate. Although

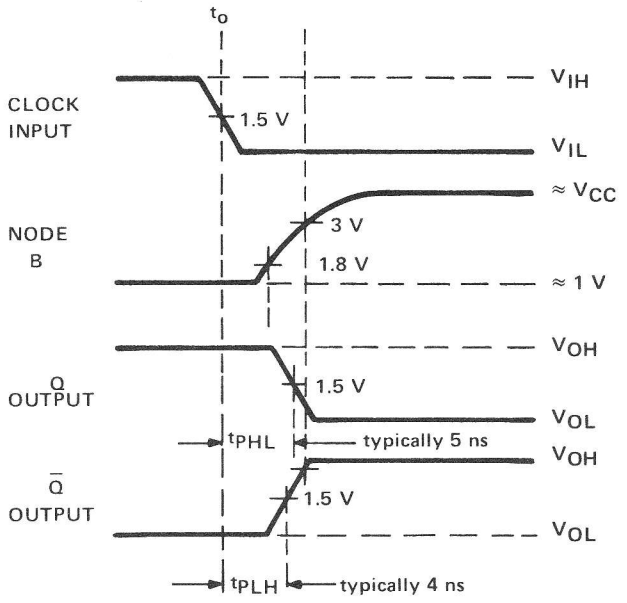


FIGURE 1.11 Timing Relationship of Flip-Flop to Clocking Transition

1.5.1 TRANSFER CHARACTERISTICS

Since the most common application for a logic gate is to drive another similar logic gate, the input and output logic levels must be compatible. The input and output logic levels for Series 54S/74S logic functions are defined as follows:

- V_{IL} – the voltage required for a low-logic level at an input. It is a guaranteed maximum of 0.8 volt.
- V_{IH} – the voltage required for a high-logic level at an input. It is a guaranteed minimum of 2 volts.
- V_{OL} – the voltage output for the low-logic-level state. It is a guaranteed maximum of 0.5 volt.
- V_{OH} – the output voltage for the high-logic-level state. It is a guaranteed minimum of 2.5 volts for Series 54S and 2.7 volts for Series 74S.
- V_T – the threshold voltage at which the input and output voltages are equal.

Typical values for these parameters are presented in Table 1.2 for TI Series 54S/74S NAND gates. These are not worst-case definitions, but typical operating values calculated from nominal valued components for a fan-out of 10. Examination of Table 1.3 reveals that these parameters, with the exception of V_{OH}, which is a direct function of

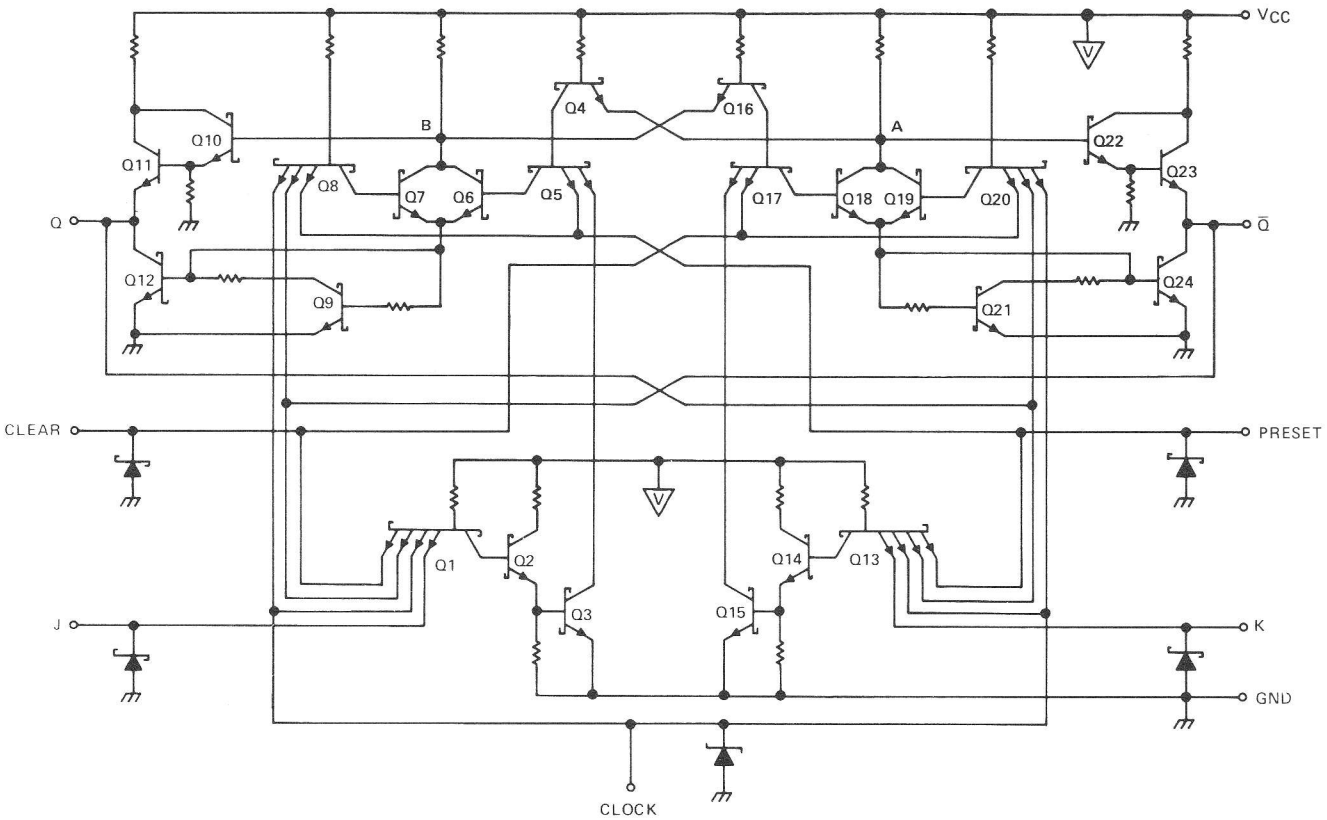


FIGURE 1.12 SN54S/74S112 Flip-Flop Schematic Diagram

most devices have characteristics close to the average values shown, some devices may vary within the data sheet limits.

V_{CC}, are virtually flat across the ambient temperature and supply voltage ranges.

Table 1.2 – Typical Output and Threshold Voltages for SN54S00/74S00 Gates*

As function of ambient temperature (T_A)

V_{CC} = 5 V, R_L = 280 Ω

	–55°C	0°C	25°C	70°C	125°C
V_{OH}	3.2	3.3	3.4	3.6	3.8
V_{OL}	0.4	0.38	0.37	0.365	0.36
V_T	1.41	1.35	1.3	1.2	1.19

As function of supply voltage (V_{CC})

T_A = 25°C, R_L = 280 Ω

	4.5 V	4.75 V	5.0 V	5.25 V	5.5 V
V_{OH}	2.9	3.15	3.4	3.65	3.9
V_{OL}	0.38	0.375	0.37	0.37	0.37
V_T	1.28	1.29	1.3	1.32	1.35

*This table is supplied to illustrate the acutal design points for the Series 54S/74S circuits, and although full-temperature typicals are shown, the guaranteed values given in the data sheet should be used for system designs.

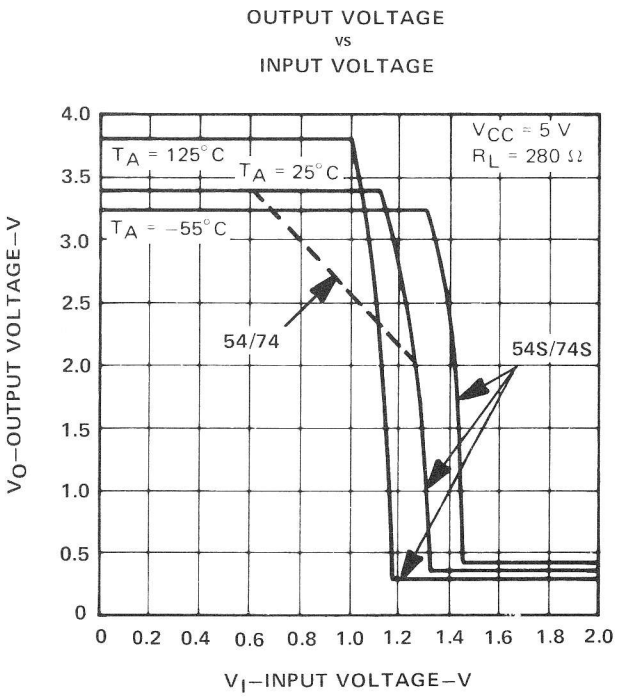


FIGURE 1.13. Voltage Transfer Characteristics of Typical TTL/STTL NAND Gate

An analysis of the input-output response characteristics of a typical Schottky-clamped TTL gate is necessary to understand the operation of this device in most system applications. From a d-c standpoint, this response can best be depicted with the use of a V_{IN}-V_{OUT} transfer plot. Figure 1.13 is a typical transfer characteristic of a Series 54S/74S gate, and for comparison purposes, the characteristic of a standard Series 54/74 gate is also shown.

The Schottky NAND gate has a transfer function which is relatively square, and therefore maintains a higher logic 1 level than the standard gate between input voltages of 0.6 and 1.3 volts. This improvement in the logic-1 level noise immunity is the result of replacing the passive (resistor) turn-off circuit between the base and emitter of the output transistor of a standard gate with an active turn-off circuit (Q5, Figure 1.10).

Figure 1.13 also examines in more detail the d-c transfer characteristics of the Series 54S/74S NAND gate at –55°C, 25°C, and 125°C. The guaranteed noise immunities may be calculated as follows:

Guaranteed high-logic-level noise immunity = V_{OH} MIN – V_{IH} MIN

Guaranteed low-logic-level noise immunity = V_{IL} MAX – V_{OL} MAX

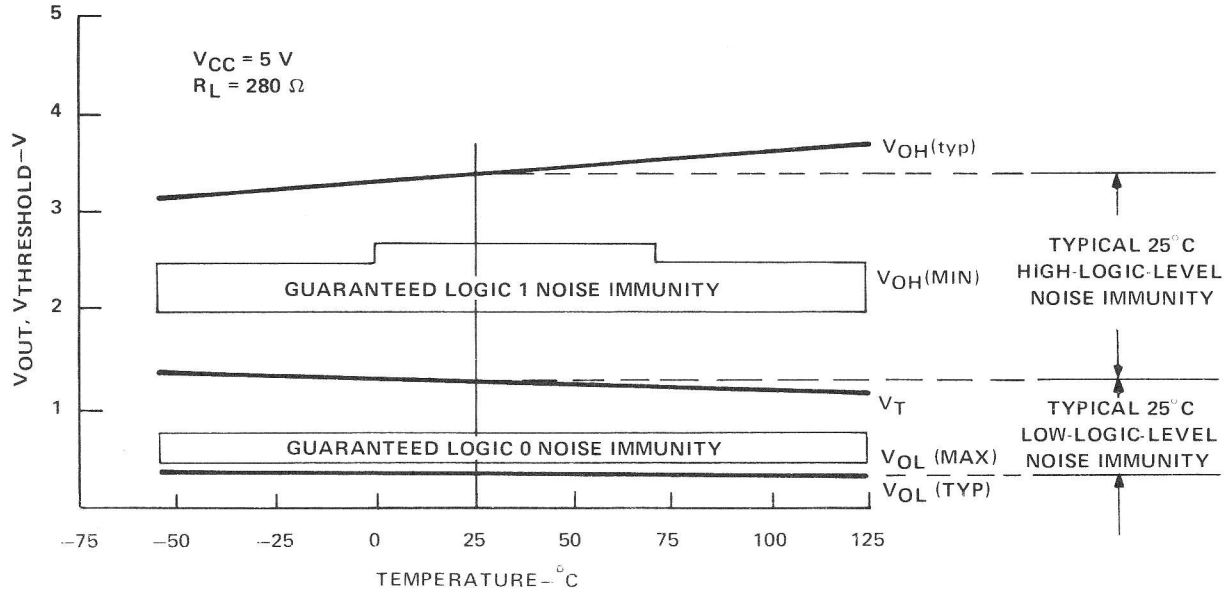


FIGURE 1.14. V_O and V_T versus Temperature

For a Series 74S device, the guaranteed noise immunities are 700 millivolts and 300 millivolts respectively, and for a Series 54S device, the guaranteed immunities are 500 millivolts and 300 millivolts respectively. Typically, however, the noise margins are much greater than the minimum guaranteed. From Figure 1.14, it can be seen that the worst-case high-logic-level noise immunity occurs at low temperature, but at $-55^{\circ}C$, it is still typically about 1.8 volts. At $125^{\circ}C$, the worst-case temperature for low-logic-level noise immunity, the typical noise margin is 0.8 volt.

1.5.2 INPUT CHARACTERISTICS

Knowledge of the input and output characteristics of a Series 54S/74S gate is required to utilize these devices fully. This knowledge is particularly necessary when a device interfaces with something other than Series 54S/74S TTL elements. For example, the expression "fan-out of 10" has no meaning when anything but similar Series 54S/74S gates are being driven. Knowledge of the voltage-current relationships for all elements involved is important for proper design.

Figure 1.15 illustrates typical input current (I_I) versus input voltage (V_I) characteristics for a Series 54S/74S TTL gate input during normal operation. A typical Series 54/74 characteristic is also shown for reference. Any device used to drive a TTL gate must source and sink current. Conventionally, current flowing toward a device terminal is designated as positive, and current flowing away is negative. Thus, I_{IL} is negative current because it flows out of the input terminal, and because I_{IH} flows into the input terminal, it is positive.

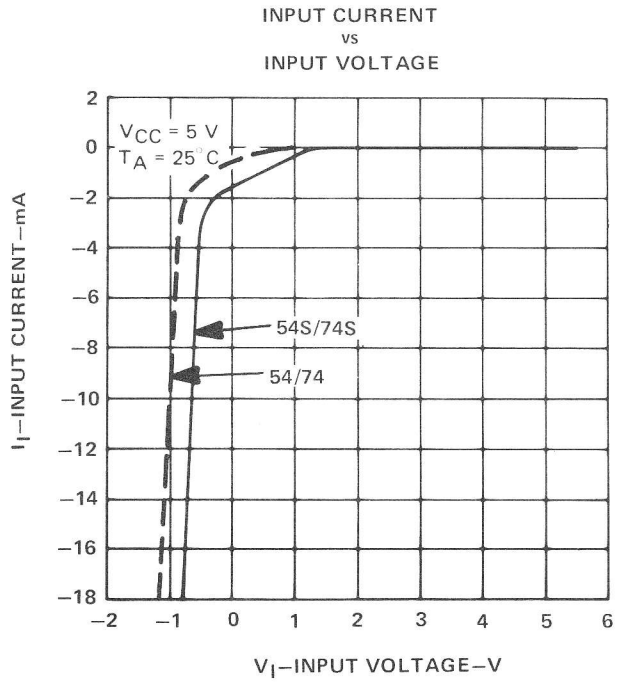


FIGURE 1.15 I_I versus V_I

1.5.2.1 Low-Level Input Current

Figure 1.16 depicts the d-c equivalent of a standard Series 54S/74S input circuit showing the input current paths. During a low-logic-level-input state ($V_{IL} \leq 0.8$ volt),

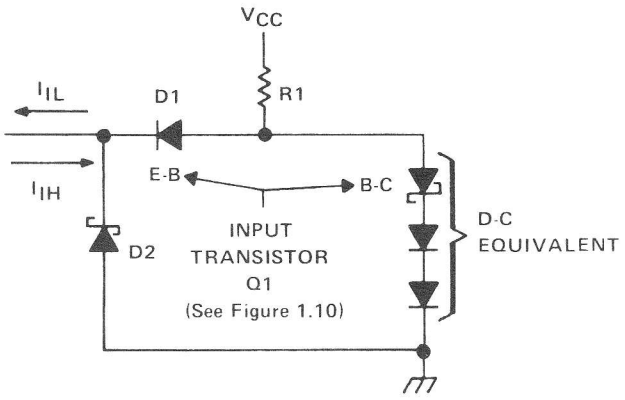


FIGURE 1.16 Equivalent D-C Circuit for STTL Input

the input current I_{IL} is primarily determined by resistor R1. However, I_{IL} is also a function of the supply voltage V_{CC}, the ambient temperature T_A, and the input voltage V_{IL}.

To assure desired device operation under all possible conditions, the worst-case test is performed on all devices. Note that V_{CC} is taken to its highest allowable value to maximize I_{IL}. With the exception of the input under test, all unused inputs are taken to a high-logic level to maximize any contribution of these inputs to I_{IL} of the emitter under test. Thus, acceptable Series 54S/74S gates of one unit load have $I_{IL} \leq |-2|$ milliamperes at $V_I = 0.5$ volt. This maximum current is a low-logic-level load of N = 1 for a gate output.

Steady state input voltages below ground (0 volt) will experience increasing input current at a linear rate until the Schottky input clamping diode becomes forward biased. At this point, approximately −0.4 volt, input current increases rapidly. The low forward impedance input clamping diodes are intended to clip negative undershoot resulting from the fall time of an a-c input signal, and as such there are no restrictions for operation at standard input voltage levels.

1.5.2.2 Input Clamping Diode Tests

The quality of the input clamping SBD (D2, Figure 1.16) is tested by ensuring that the forward voltage drop is no more than −1.2 volts with a forward current of −18 milliamperes. These values are guaranteed at V_{CC} = MIN and are valid across the operating temperature range. The characteristic of the input diode is illustrated in Figure 1.17 across the temperature range and at −10, −18, and −25 milliamperes of current. The typical forward voltage drop of a Series 54/74 input clamping diode is shown for reference.

1.5.2.3 High-Level Input Current

Another input parameter that must be measured and controlled is input current at the high-logic level, I_{IH}. When

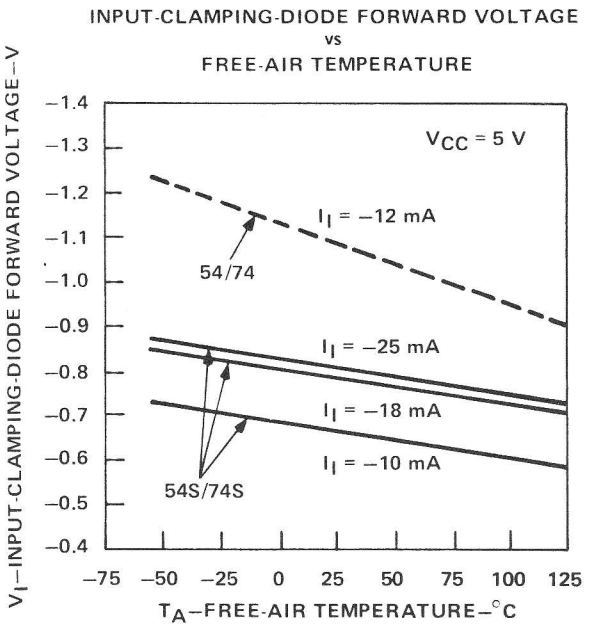


FIGURE 1.17 Input-Clamping Diode Forward Voltage versus Temperature

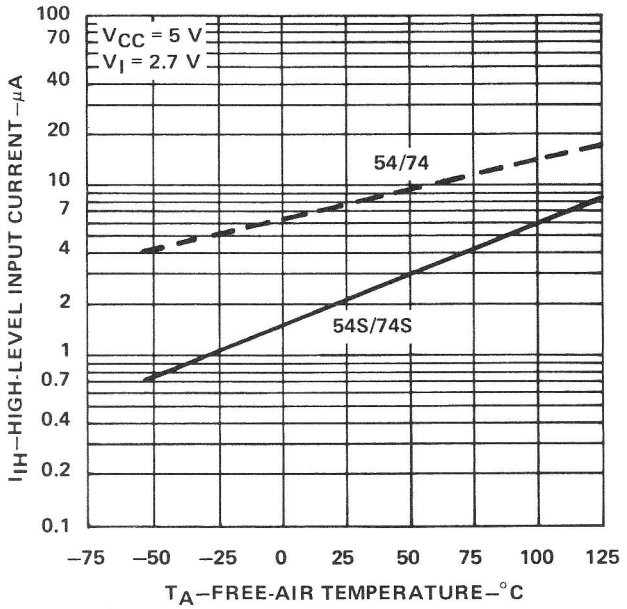


FIGURE 1.18 High-Level Input Current versus Temperature

all inputs of a multiple-emitter Series 54S/74S TTL gate are at a high-logic level, the emitter-base (EB) junction is reverse biased, and the collector-base (BC) junction is forward biased. Thus, an emitter acts like a collector, and a collector acts like an emitter. Input current now is a function of the inverse current gain $h_{FE(inv)}$ of the input transistor Q1 (see Figure 1.10). However, if one or more of the input emitters is at a low-logic level, inverse transistor action between emitters, or emitter-to-emitter leakage, may occur in addition to, or in place of, the inverse transistor action between the high-logic-level emitter and the collector. Thus, I_{IH} current may split into several currents inside the TTL gate.

To assure desired device operation under all possible conditions, the worst-case test is performed with all unused inputs grounded, and V_{CC} maximized to provide the highest level of I_{IH} current. This arrangement also maximizes base-current drive for inverse h_{FE} within specified operating conditions. The real concern is to screen out those devices with an I_{IH} of sufficient magnitude to cause a degradation of V_{OH} at an output (which happens to be driving 20 such inputs). An $I_{IH} \leq |50|$ microamperes measured with V_I at 2.7 volts is acceptable for a unit load input. Typical values are plotted against temperature in Figure 1.18. Again, a typical Series 54/74 I_{IH} is shown for reference.

1.5.2.4 Input Breakdown Tests

An additional I_{IH} test is performed to check for input emitter breakdown voltage. A breakdown voltage test at 5.5 volts is performed to assure that an input emitter-base junction will not be damaged if a voltage source up to 5.5 volts (maximum recommended V_{CC} for Series 54S/74S devices) is applied to a gate input. The emitter-base junctions of a Series 54S/74S TTL gate are physically very small, and may be damaged if too much power is dissipated in the junction.

From this discussion, it should be apparent that each input of a multiple-emitter TTL gate represents a load of 1 (N = 1) in both logical states. A low-logic-level input load is $I_{IL} \leq |-2|$ milliamperes at V_{IN} = 0.5 volt. A high-logic-level input load is $I_{IH} \leq |50|$ microamperes at V_{IN} = 2.5 volts.

The following guidelines should be observed with respect to the specification of an input voltage condition when interfacing with non-TTL signals or when terminating unused inputs:

a) The instantaneous voltage differential applied at two emitter-inputs of a multiemitter input transistor should not exceed 5.5 volts.

b) The instantaneous voltage differential $[V_{I(max)}]$ applied between any input (single or multiemitter) and ground (GND) should not exceed 5.5 volts.

1.5.2.5 Equivalent A-C Impedance of Inputs

Dynamically, the STTL input includes a lumped capacitance (C) of approximately 3 picofarads which is made up of the package lead, bond wire, the base-emitter junction, and the clamping diode D2. The effects of this capacitance are illustrated in Figure 1.19, and the magnitudes are:

$$Q_H \geq C\,(V_T - V_{IL}) \text{ when D1 stores}$$

$$Q_L = C\,(V_T - V_{IL})$$

The storage of D1 is minimized as the input transistor is Schottky clamped, and for all practical purposes $Q_H \cong Q_L$.

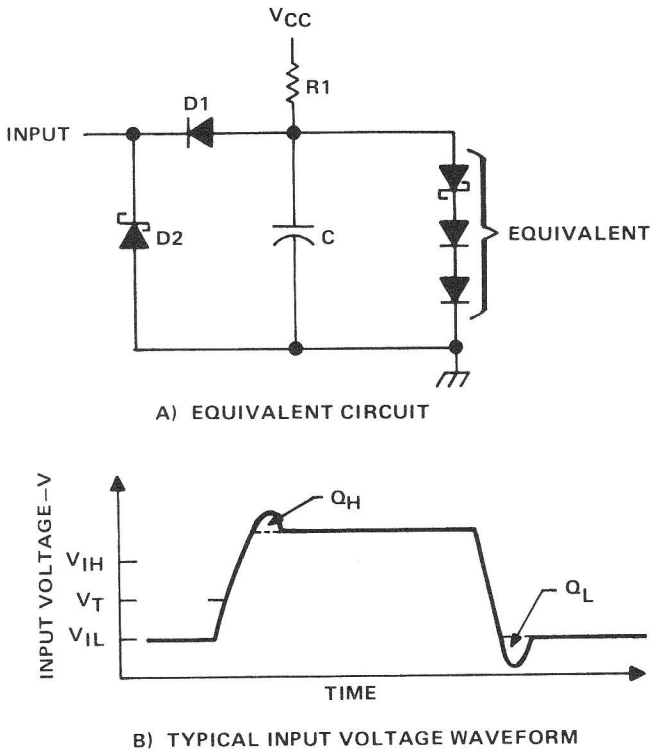


FIGURE 1.19 Equivalent A-C Circuit and Input Waveform

The STTL input is not a fixed impedance input and should not be considered as such, especially when it is the receiver on a transmission line. Analysis of line driving/receiving in Section 2 shows that the STTL input is superior to a fixed impedance input.

1.5.2.6 A-C Noise Immunity

System noise discussed in detail in Section 2, rarely occurs in strictly d-c level shifts but rather as pulses of varying duration. Noise pulses with widths greater than the propagation delay of a device may be considered as d-c noise and if they are of sufficient amplitude, will be recognized and propagated by the device. However, as the noise pulse width decreases below the propagation time of the device, the ability of the device to reject the noise improves. Illustrated in Figure 1.20 is the required pulse amplitude for a given pulse width before it will be propagated by a Series 54S/74S NAND gate.

1.5.2.7 Schmitt-Trigger Input Thresholds

A device which has even less sensitivity to input noise than the standard NAND gate is the Schmitt trigger. The SN54S/74S132 Schmitt trigger performs the NAND function but the input threshold has the unique characteristic of hysteresis. This hysteresis, the most important feature of a Schmitt trigger, is generated by the difference in the positive-going (V_T+) and the negative-going (V_T-) thresholds. Threshold V_T+ is the high-level input voltage which must be achieved before the output switches from a high to a low voltage and threshold V_T- is the low-level voltage to

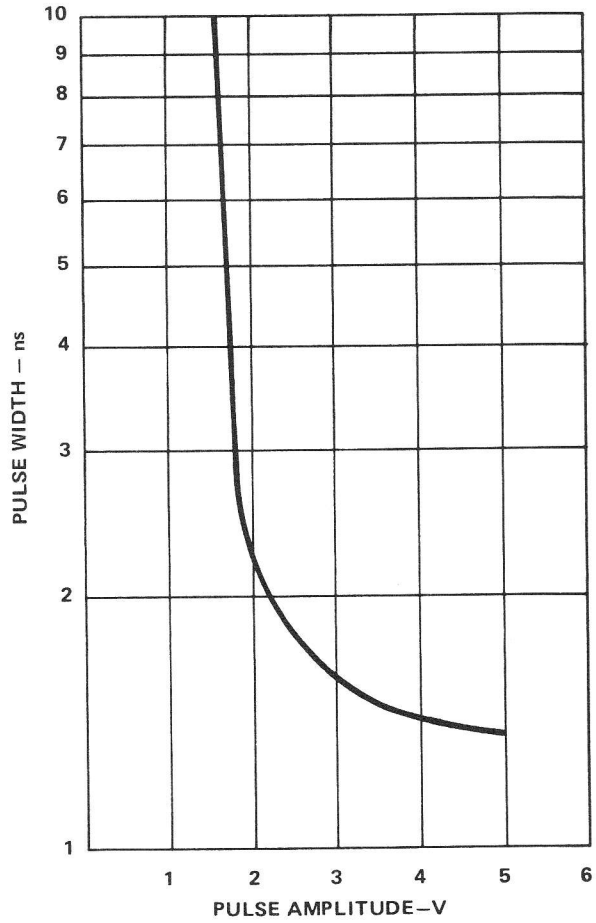


FIGURE 1.20 Noise Pulse Width versus Pulse Amplitude for STTL Gate

which the input must drop before the output switches from a low to a high voltage. The typical transfer characteristic for the SN54S/74S132 is shown in Figure 1.21. At 25°C, V_T+ is 1.77 volts and V_T- is 1.22 volts, producing typically 550 millivolts of hysteresis. The benefit of this hysteresis is examined in Figure 1.22 by comparing the

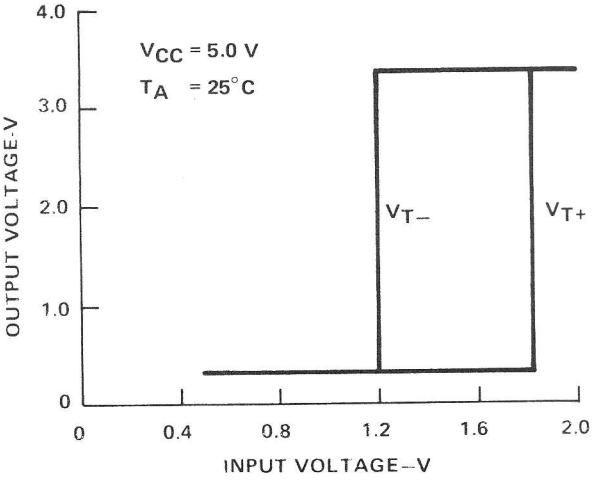


FIGURE 1.21 Transfer Characteristic of SN54S/74S132

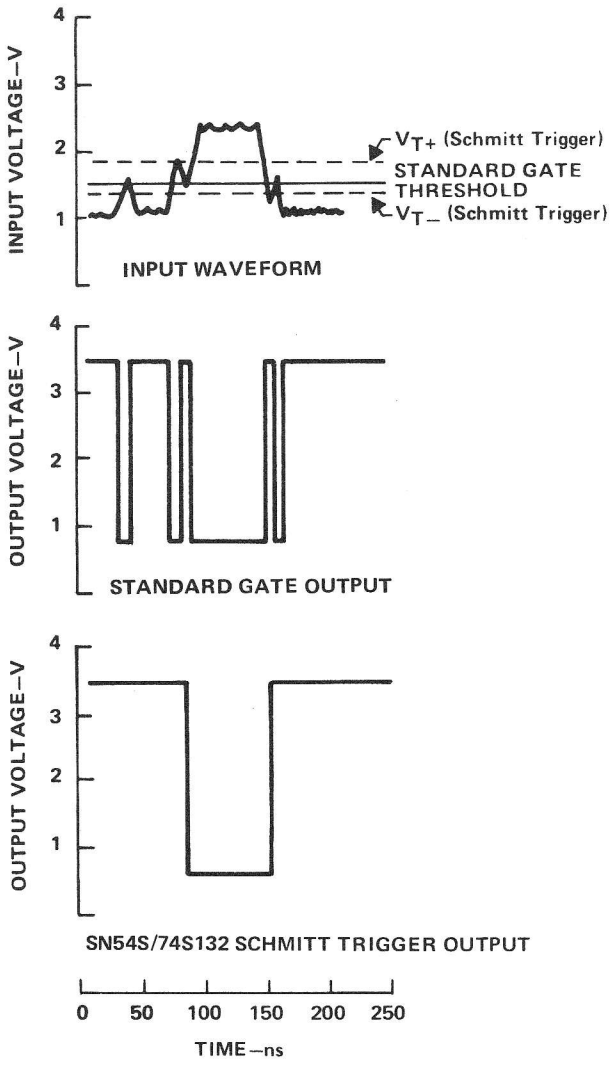


FIGURE 1.22 Response of Standard Gate and Schmitt Trigger to Noisy Input

output response of the Schmitt trigger and the response of a standard NAND gate to a noisy input signal.

As the result of a single input threshold, the standard gate changes logic levels each time the input signal passes through its threshold and, in this particular case, would generate data which included the noise spikes; while the Schmitt trigger, with hysteresis, did not respond to the noise spikes and generated a clean waveform.

1.5.3 OUTPUT CHARACTERISTICS

The most versatile type of STTL output is the double-ended, totem-pole as it demonstrates a low-impedance drive capability for both high-logic-level and low-logic-level loads. Included in the STTL family are four basic double-ended outputs:

a) The standard fan-out output features a Darlington pair for driving 20 high-level loads and a high-sink-current transistor for driving 10 low-logic-level loads at ≤ 0.5 volt when on.

b) A buffer/clock driver has the same output configuration but features improved high- and low-level drive capabilities for fanning out to 60 high-logic-level and 30 low-logic-level loads.

c) A line driver, the SN54S/74S140, with the same type of output as the SN54S/74S40, features an improved high-logic-level output for driving 50-ohm lines. It also sinks 60 milliamperes at ≤ 0.5 volt.

d) A bus-buffer output on some device types features a third or high-impedance state which neither loads nor drives the bus significantly. This type of output has the same type of double-ended drive but a number of outputs can be connected to a common bus if system controls are organized to ensure that all but one of the common outputs are off (in the high-impedance state).

1.5.3.1 High-Level Output Characteristics

The ability of the totem-pole output to supply high-logic-level output current is parametrically tested by forcing an I_{OH} value during measurement of V_{OH}. However, the quality of the components supplying the I_{OH} (Darlington pair and 50-ohm resistor) is best indicated by parametrically measuring their current-sourcing (I_{OS}) capability when shorted directly to ground. As an example, units exposed to the V_{OH}/I_{OH} test can pass with series resistances as shown in Table 1.4. However, in order to pass the I_{OS} test, the total series resistance can be no more than that shown in the right-hand column of Table 1.3.

Table 1.3 – D-C High-Level Output Impedance of STTL Totem-Pole

	V_{OH}/I_{OH} Testing		I_{OS} Testing	
	Voltage Drop $(4.75-V_{OH}) : I_{OH}$	Max Series Resistance To Pass	$(V_{CC}-0) : I_{OS}$	Max Series Resistance to Pass
SN74S00	2.05 V at 1 mA	2050 Ω	5.25 V at 40 mA	131.25 Ω
SN74S40	2.05 V at 3 mA	683 Ω	5.25 V at 50 mA	105 Ω
SN74S134	2.35 V at 6.5 mA	361 Ω	5.25 V at 40 mA	131.25 Ω
SN74S140	2.75 V at 40 mA	69 Ω	V_{OH}/I_{OH} guarantees	69 Ω

Primarily then, this test ensures that the output possesses the high capacitive drive capability, which is typical of the TTL totem-pole output. And, the maximum I_{OS} also guarantees current-limiting, which ensures that device damage will not occur under normal use or trouble-shooting conditions. The typical V_{OH} versus I_{OH} is shown in Figure 1.23 and compared to the standard Series 54/74 output.

Figure 1.23 shows that the high-logic-level output drive circuit consists primarily of the Darlington pair and resistors R2 and R4. The high-logic-level output voltage follows changes in the supply voltage practically volt for volt.

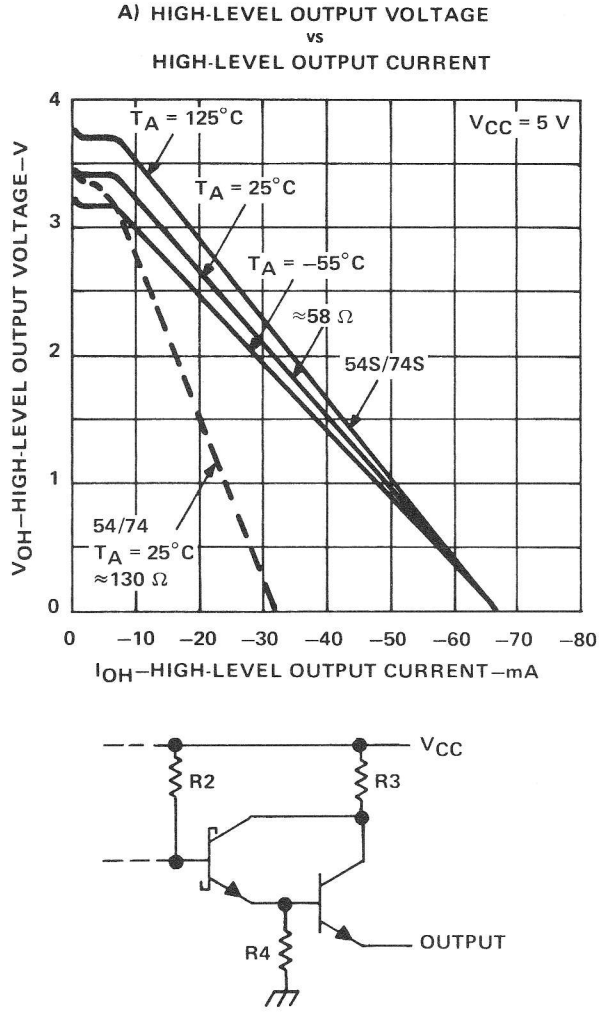


FIGURE 1.23 Series 54S/74S V_{OH} versus I_{OH} and Equivalent Schematic

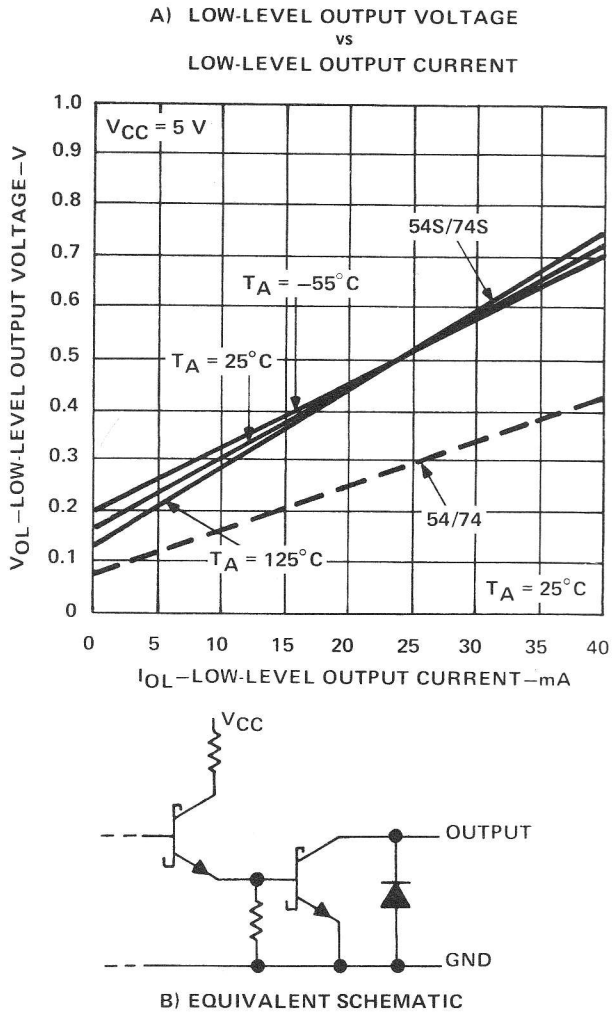


FIGURE 1.24 Series 54S/74S V_{OL} versus I_{OL} and Equivalent Schematic

When measuring worst-case high-logic-level output voltage, the minimum supply voltage is used. A worst-case low-logic-level input voltage (0.8 volt) is applied to an input, and unused inputs are tied to the V_{CC}. This situation represents worst-case conditions, since this high voltage from V_{CC} would tend to turn on the transistors if it were not for the low-level input. Since the gate was designed to drive 20 Series 54S/74S input high-logic level loads, it must source −1 milliampere at V_{OH} minimum to pass this test.

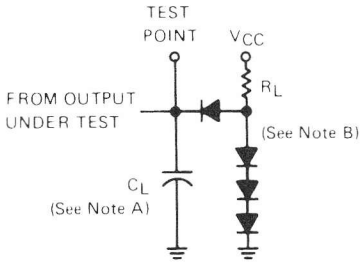
1.5.3.2 Low-Level Output Characteristics

Figure 1.24 depicts that section of the output drive circuit which produces a logical 0 output voltage V_{OL}. The minimum supply voltage is used for worst-case testing of V_{OL}. At the same time, all inputs are connected to the minimum high-logic-level input voltage (2.0 volts). Since the basic gates were designed to drive 10 Series 54S/74S low-level input loads, the output must sink 20 milliamperes at $V_{OL} \leq$ 0.5 volt ($I_{IL} \leq |-2|$ milliamperes at V_{OL} = 0.5 volt to pass this V_{OL} test. A typical Series 54/74 fan-out of 10 output is shown for reference. The increased on-level voltage for the Series 54S/74S output is a result of the Schottky clamping diode which bypasses excess base drive and eliminates storage of the output transistor.

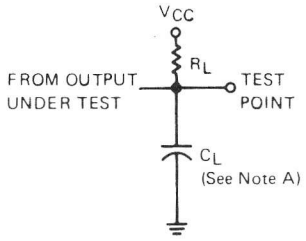
1.5.4 SWITCHING SPEED

Two switching-time parameters are guaranteed on TI Series 54S/74S TTL gates: propagation delay time for a high-logic-level to a low-logic-level at the output (t_{PHL}), and propagation delay time from a low-logic level to a high-logic level at the output (t_{PLH}). Both parameters are specified with respect to the input pulse, using the test conditions of Figure 1.25. The diodes and resistor R_L, are used to simulate the d-c loading of worst-case Series 54S/74S loads. Typical switching times are provided for a capacitive loading (C_L) of 50 picofarads approximating 10 Series 54S/74S inputs plus about 20-picofarad wiring capacitance, and of 15 picofarads, approximating lighter loading for speed-critical paths. Maximum times are guaranteed for the 15 picofarad load. The switching tests are performed at nominal operating conditions: V_{CC} = 5 volts and T_A = 25°C. Acceptable SN54S00/SN74S00 devices have $t_{PHL} \leq$ 5 nanoseconds and $t_{PLH} \leq$ 4.5 nanoseconds with the 15 picofarad load. Under these conditions, a

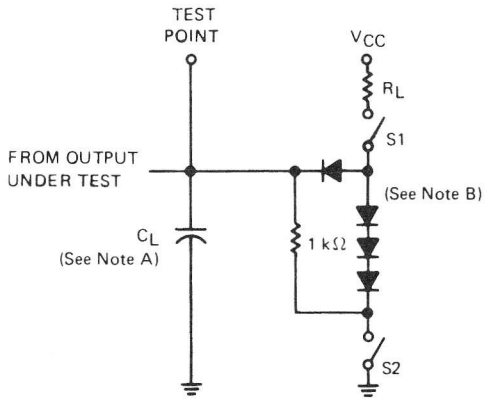
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

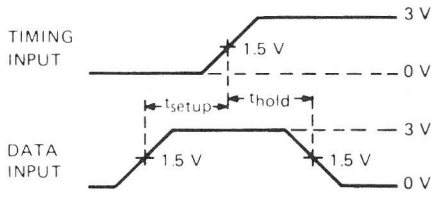


LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

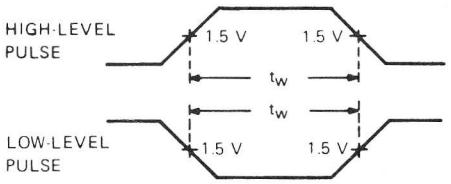


LOAD CIRCUIT FOR THREE-STATE OUTPUTS

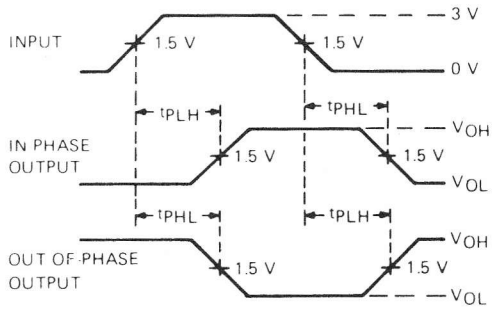
NOTES. A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.



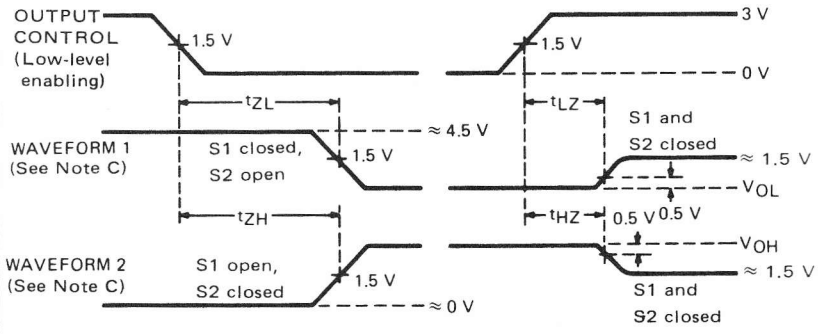
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

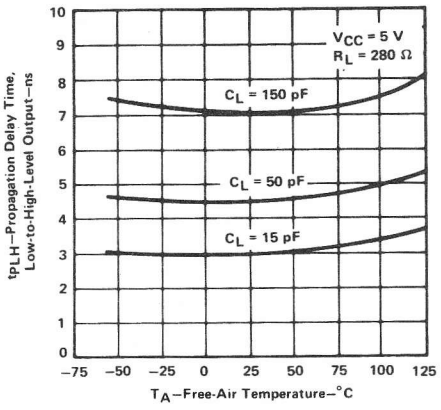
NOTES: C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$ and:
For Series 54/74 and 54H/74H, $t_r \leq 7$ ns, $t_f \leq 7$ ns;
For Series 54S/74S, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

FIGURE 1.25 A-C Load Circuits and Voltage Waveforms

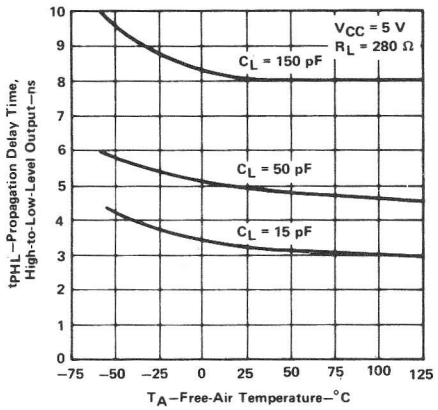
typical device will have t_{PHL} and $t_{PLH} \approx 3$ nanoseconds. Typical switching times as a function of ambient temperature and supply voltage are shown in Figure 1.26 and 1.27 at various load conditions. Note that both t_{PHL} and t_{PLH} vary little with temperature changes.

TYPICAL SWITCHING CHARACTERISTICS†

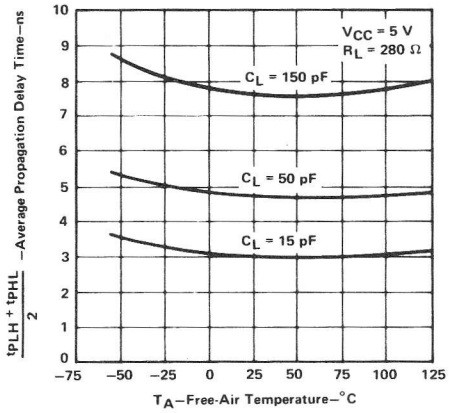
NAND GATE PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE†



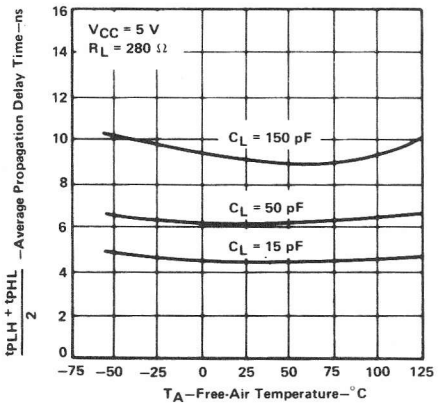
NAND GATE PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT§
vs
FREE-AIR TEMPERATURE†



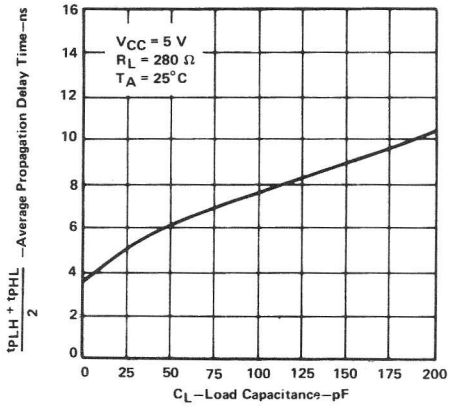
AVERAGE NAND GATE PROPAGATION DELAY TIME §
vs
FREE-AIR TEMPERATURE†



FLIP-FLOPS
'S112, 'S113, 'S114
AVERAGE PROPAGATION DELAY TIME,
CLOCK TO OUTPUT
vs
FREE-AIR TEMPERATURE†

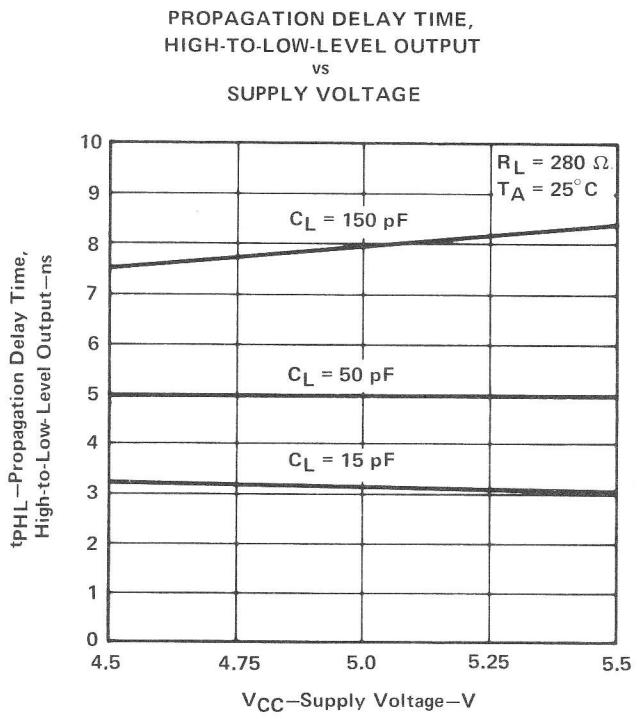


FLIP-FLOPS
'S112, 'S113, 'S114
AVERAGE PROPAGATION DELAY TIME,
CLOCK TO OUTPUT
vs
LOAD CAPACITANCE



† Data for temperatures below 0°C and above 70°C are applicable for Series 54S circuits only.
§ Data as shown are applicable specifically for the NAND gates with totem pole outputs.

FIGURE 1.26 Switching Times versus Free-Air Temperature



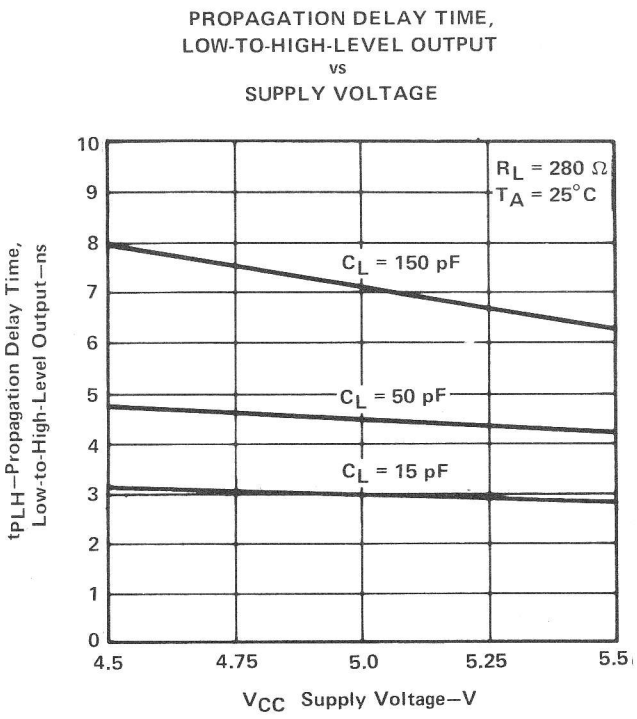


FIGURE 1.27. Switching Times versus Supply Voltage

1.5.5 SUPPLY CURRENT CHARACTERISTICS

Power-supply current requirements for all Series 54S/74S circuits are specified as maximum current drains at maximum permissible power-supply voltage, V_{CC}. These are worst-case static d-c tests and for gates are performed separately with the output low, and with the output high. For flip-flops and MSI devices, the I_{CC} test is performed under specified conditions which produce the maximum current.

Since Series 54S/74S gate packages contain different numbers of gates (one, two, three, four, or six), the supply current required by various types will be a function of the number of gates in the package. A normalized per-gate value of supply current is shown on the data sheet for most SSI types and total supply current is obtained by multiplying this value by the number of gates. Of course, all gates within the package are assumed to be in the same logic state.

With the supply voltage at 5 volts, typical I_{CCL} and I_{CCH} values per gate are also shown on the data sheet as well as an average-per-gate value, which assumes a 50% duty cycle.

When power-supply currents are specified at the nominal V_{CC} (5 volts), the true worst-case current drain is not obtained. I_{CC} at nominal V_{CC} is, in fact, approximately only 91% of the worst-case value, and the resulting power dissipation is approximately 82% of the worst-case value.

The currents mentioned above are for static d-c conditions only. When a Series 54S/74S TTL gate or any gate with a totem-pole output switches from the logical 0 state to the logical 1 state, a momentary increase in supply current occurs. With no load on the output, this increased supply current is a function of internal capacitance and output overlap. The reduced overlap of the Series 54S/74S output shortens both the duration and resultant amplitude of the internal current. In addition, any capacitance connected to the output must be charged and discharged as the gate output switches. When an output switches from low to high, system load capacitance connected to the output must be charged by I_{CCH} current. This charging current is directly related to the system load capacitance; however, as Figure 1.26 illustrates, the low-impedance output provides sufficient drive to charge the capacitance rapidly. Figure 1.28 illustrates the effect of device switching frequency on the average supply current (and thus power dissipation of the gate). Additional data is provided in paragraph 2.3.3.

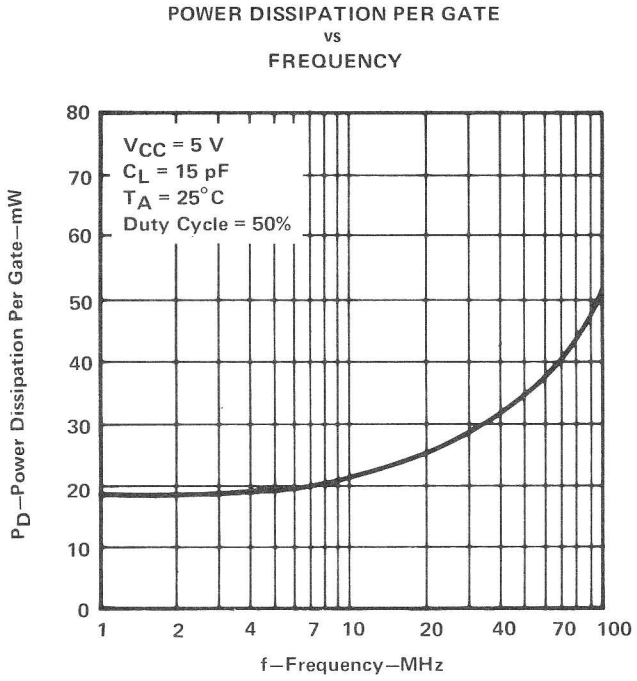


FIGURE 1.28 Typical Power Dissipation/Gate versus Frequency

1.5.6 D-C NOISE MARGINS

D-C noise margin is defined as the difference between the guaranteed logic state voltage limits of a driving gate and the voltage requirements of a driven device. The area of safe operation, commonly called guaranteed d-c noise margin, is illustrated in Figure 1.14. The principal motivating factor in setting up the test conditions is to guarantee the user an absolutely safe operating margin, as pointed out in the earlier descriptions and discussions on d-c testing of Series 54S/74S devices.

Outputs are guaranteed over the worst-case temperature and V_{CC} not to exceed 0.5 volt for a low-level output or fall below the V_{OH} minimum. However, when voltages are applied to the input to obtain these output conditions, 2 .0 volts is used as a high-level input and 0.8 volt is used as a low-level input. A guaranteed worst-case margin for both logic states results. In the high logic state, the Series 74S output will not go below 2.7 volts, but the driven gate requires an input voltage of no more than 2.0 volts before significant output voltage change occurs. A 700-millivolt V_{CC} noise excursion is then possible without propagating the noise through subsequent stages.

1.5.7 NOISE REJECTION

The ability of a logic element to operate in a noise environment involves more than the d-c or a-c noise margins discussed in paragraph 1.5.2. To be a problem, an externally generated noise pulse must be received into the system and cause a malfunction. Stable logic systems with no storage elements are practically impervious to a-c noise, although large d-c voltages could cause trouble. Systems with triggerable storage elements, or those operating fast enough for the noise to appear as a signal, are much more susceptible.

The noise voltage must be introduced into the circuit by radiated or coupled means. The amount of noise required to develop a given voltage is strictly a function of the circuit impedance. It is in this way that the low output impedances of TTL improve noise immunity. Noise must be transferred from the noise source, with some arbitrary impedance, through a coupling impedance to the impedance of the circuit under consideration.

A typical circuit where the coupling impedance is stray capacitance, and the load impedance is provided by gates, is shown in Figure 1.29. In relatively tight coupling

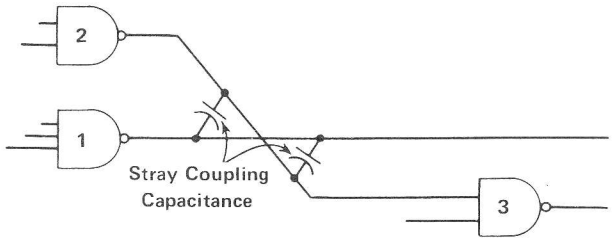


FIGURE 1.29 Stray Coupling Capacitance

such as this, the loading effect on the driving source is significant enough to be considered. However, since th source effect is difficult to assess and is in a direction to improve rather than degrade the noise rejection, its effects will be ignored, resulting in a worst-case type of response indication. Also, in the case of radiated noise, the source resistance is definitely a factor in noise coupling, essentially replacing the reactive coupling impedance.

Thus ignoring the driving source impedance to make the conditions more nearly standard, it is possible to determine a set of curves relating the developed noise pulse to the noise source amplitude, the noise rise (or fall) time, the coupling impedance, and the load impedance. Such curves have been developed by Elmore and Sands[1] for several different input waveforms. The type that is most applicable is the ramp input, since the STTL wavefront is essentially a ramp with a dv/dt of 1 volt per nanosecond.

Figure 1.30(a) shows the equivalent circuit from which the plot of Figure 1.30(b) was developed. The input pulse (shown as a heavy line) is a step signal with a linear rise, requiring unit time (normalized), and the output pulse is represented analytically by

$$e_0 = \tau(1 - e^{-t/\tau})$$

$$\tau = RC$$

with holding for unit time. This is followed by an exponentially decaying voltage having a time constant τ. Values of τ and t on the figure are normalized by the value of the total rise time of the simulated noise pulse e_i. Using

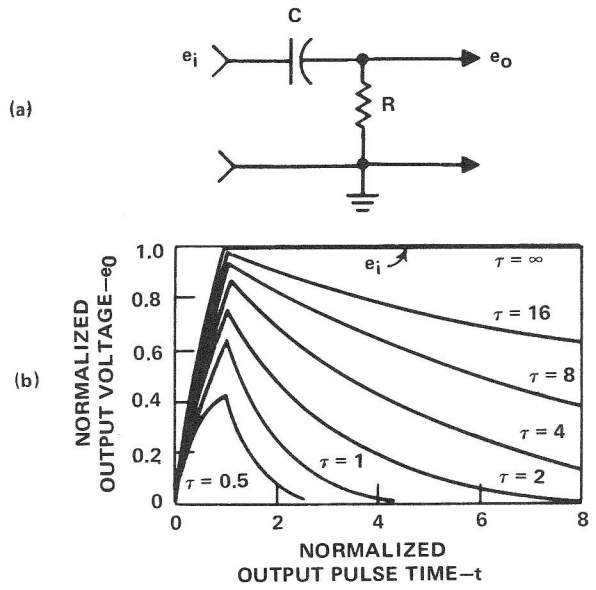


FIGURE 1.30 Evaluations of Gate Response to Ramp/Amplitude of Input

Figure 1.30(b), it is possible to determine the pulse width and amplitude of the coupled noise pulse.

As an example, allow a pulse of 3-volt amplitude rising at 1 volt per nanosecond with gate 2 output (Figure 1.29) in the high logic state. Assume the nominal 58-ohm output impedance and 10 picofarads of coupling capacitance.

$$\tau = RC = (10 \times 10^{-12})(58) = 0.58 \times 10^{-9} = 0.58 \text{ ns}$$

$$\text{Total rise time} = \frac{3 \text{ V}}{1 \text{ V/ns}} = 3 \text{ ns}$$

Now to convert the normalized values of τ and t of Figure 1.30(b) to actual values, multiply by 3 nanoseconds. The output voltage scale will be multiplied by 3 volts. Using the $\tau = 1$ curve gives a peak e_o of 1.5 volts (0.5 X 3) and a pulse width of 3 nanoseconds at the 50% points. To determine whether or not this pulse will cause interference, these values (1.5 volts and 3 nanoseconds) are entered on the graph of Figure 1.20. Since the gate has about 1.8 volts noise immunity at this point, the gate will not be affected.

If an open-collector gate such as the SN54S03/SN74S03 were to be used with a passive 1 kilohm pull-up, the picture would change:

$$\tau = (10 \times 10^{-12})(1 \times 10^{3}) = 10 \times 10^{-9} = 10 \text{ ns}$$

$$\text{Total rise time} = \frac{3 \text{ V}}{1 \text{ V/ns}} = 3 \text{ ns}$$

Now the amplitude (from the curves) approaches 3 volts (0.96 X 3) and the pulse width at the 50% points is approximately 10 nanoseconds (1 X 10). Gate 3 (Figure 1.28) will certainly propagate this pulse.

This is obviously an oversimplification. The coupling impedances are complex (but resolvable into RLC series coupling elements) and the gate output impedance changes with load. But our purposes are to show why and how the low impedance of the active TTL output rejects noise and to facilitate a comparison with the passive pull-up.

The ability to operate in a noisy environment is an interaction of the built-in operating margins, the time required for the device to react, and the ease with which a noise voltage is developed. In all except the ability to react to short noise pulses, if developed, TTL design has emphasized noise rejection.

So far nothing has been said about noise in devices other than gate circuits. Many MSI devices are complex gate arrays, and because of their small size, they are superior in noisy environment operation to their discrete gate equivalents. Noise tolerance of latching devices is implied in the setup times, hold times, clock pulse width, data pulse widths, and similar parameters. Output impedances and input noise margins are quite similar to those of the gates and may be treated similarly. A point to be remembered is that if a latching device does become noise-triggered, the effective error is stored and does not disappear with the noise. More detailed analysis of system noise is provided in paragraph 2.3.

2.0 GUIDELINES FOR SERIES 54S/74S SCHOTTKY TTL SYSTEM DESIGN

System layout and design requirements for Schottky TTL circuits are essentially the same as those guidelines which have previously been established and are applicable for all high-performance digital systems. A series of brief recaps is provided in Table 2.1 which summarizes the solutions for most design decisions needed to implement systems utilizing Schottky TTL. The recaps reference supplementary data which may be useful for developing specific answers to unique problems.

2.1 Power Supply Regulation

Power supply regulation is often treated as though it were an independent characteristic of devices involved. As a practical matter, however, power supply regulation, along with temperature range, is intimately related to noise margins, fan-out, speed, and several other variables. The characteristics most affected are noise margin and fan-out, and generally speaking, so long as these two parameters are adequate, the power supply will be within allowable limits. Of course, on a comprehensively specified device, such as any TTL part, some auxiliary parameter, such as allowable input current out of the device, may and usually does require a more restrictive power supply range.

Generally speaking, operating a little outside the allowable limits for TTL is not disastrous. The part may not meet the specification sheet guarantees, but it should continue to operate satisfactorily. Of course, noise margin and/or some other parameter may be affected and this, combined with high ambient noise levels and extreme temperatures, may cause failures which appear to be directly related to power supply regulation.

Application of supply voltage value above 7 volts (absolute maximum rating) may result in catastrophic or degradational damage to the circuit.

Some specific characteristics directly related to the supply voltage are:

a) The V_{OH} value which tracks, almost directly, any change in the V_{CC}. In other words, if V_{CC} drops from 5.0 volts to 4.8 volts, the V_{OH} will drop approximately 200 millivolts. Conversely, an increase in V_{CC} value will result in an increased V_{OH}. Schottky TTL circuits have increased high-logic-level noise margins (500 millivolts for Series 54LS, 54S, and 700 millivolts for Series 74LS, 74S) to further suppress the effects of V_{CC} noise or ripple. In fact, none of the guaranteed noise margin is lost if V_{CC} is maintained above the *minimum* specificed on the data sheet (4.5 volts for Series 54LS, 54S and 4.75 for Series 74LS, 74S).

b) Maximum supply voltages (5.5 volts for Series 54LS, 54S and 5.25 volts for Series 74LS, 74S) are specified as a means of providing more than adequate margin to ensure that the functional capability and long-term reliability are not jeopardized. Directly affected are the power dissipated in the package and the I_{OS} value. Specifications comprehend that V_{CC} may be at a maximum value. Therefore, I_{OS} is tested at maximum V_{CC}, and package thermal characteristics, with resultant junction temperatures, are considered at maximum V_{CC} when the supply current specifications are set.

c) When practical, regulation or clamping of maximum V_{CC} to 5.5 volts, including ripple and noise spikes, can be advantageous, as then, unused inputs of AND/NAND gates can be tied directly to the supply voltage.

2.2 Power Supply Ripple

Ripple, with some exceptions, is substantially covered by the power supply regulation specification. In other words, the d-c and a-c deviation from the norm should be within the regulation allowable for the part.

In general, ripple is simply a part of the regulation problem; however, when combined with other effects, such as slow rise times, ripple becomes much more significant. As Figure 2.1 illustrates, a TTL part responds to a signal of a specific amplitude with respect to its ground pin. As a consequence, a noise signal on the ground lead has the same effect as a noise signal on the input, except that a noise signal on the ground lead appears to be inverted in its effect on an input as shown by Figure 2.2.

As an example, let's consider what might happen in the circuits of Figure 2.3. The 2.8-kilohm source (which is effectively in parallel with the 2.8-kilohm input resistor, forming an effective 1.4-kilohm resistance) sees an apparent 0.18 milliampere a-c signal. This is due to the 0.5 volt peak-to-peak ripple on the power supply, which causes an $\approx$ 0.25 volt signal to appear on the input. The 70 picofarad capacitance slows the average input rate of rise to $\approx$ 100 nanoseconds per volt at threshold (1.3 volts at 25°C) causing the input to see an apparent extra pulse. If the source impedance is decreased, both the amplitude of the interfering signal and the rise time, a function of the 70 picofarads, decrease. The apparent resistance of the emitter-base diode is $\approx$ 30 ohms; however, this does not mean the ripple disappears, even if the source impedance is zero. The apparent input noise because of ripple on the power supply is roughly 1% of the power supply ripple. Low-frequency ripple, periods of the maximum frequency which are long compared to twice the electrical length of the power supply leads between components, appears to be varying d-c and should be treated as regulation. At such frequencies, the output of the driving gate follows the ripple and cancels the apparent effects at the driven input as shown in Figure 2.4.

2.3 Noise Considerations[5]

Few subjects are so inclusive in scope and varied in connotation as the generalized term, noise. The specific area of interest is extraneous voltages and currents in digital logic systems.

Table 2.1 Guidelines for System Design Using Series 54S/74S TTL

LINE DRIVING AND RECEIVING	
Single-wire interconnections (Paragraphs 2.3.3, 2.3.4, 2.3.5)	May be used up to approximately 12". A form of ground plane is desirable. Use point-to-point routing rather than parallel routing. If longer than 12", use a dense ground plane with wire routed as close to it as practical or twisted pair cable. Use twisted pair cable for lengths exceeding 12" but less than 6' and for all clock-line interconnections.
Coaxial and twisted pair cables. (Paragraph 2.3.5)	Design around approximately 80-100 ohms characteristic impedance. Higher impedances increase cross talk. Drive lower impedances with SN54S/74S140. a. Coaxial cable of 93 ohms impedance (such as Microdot 293-3913) is recommended b. For twisted pair cable, Nos. 26 or 28 wire with thin insulation twisted about 30 turns/foot works well.
Transmission-line ground. (Paragraphs 2.3.3, 2.3.4.3)	Ensure that transmission-line ground returns are carried through at both transmitting and receiving ends. V_{CC}-decoupling ground, device ground, and transmission-line ground should have common tie point.
Cross talk (Paragraphs 2.3.4, 2.3.5)	Use point -to-point back-panel wiring to minimize noise pickup between lines. Long unshielded parallel runs should be avoided, however, if used they should carry signals propagating in the same direction.
Reflections (Paragraph 2.3.5)	Occur when data interconnects become long enough that 2 line propagation delays are $\geqslant$ pulse transition times. Normally for Series 54S/74S TTL, this is of no concern for lines shorter than 12 inches.
Resistive pull-up (Paragraph 2.3.5)	Use $\approx$ 300 ohms resistive pull-up at receiving end of long cables for added noise margin and more rapid rise times if fan-out of driving output permits.
Gates as line drivers (Paragraph 2.3.5)	Use SN54S/74S140 when driving lines with multiple loads at TTL levels.
Gates as line receivers (Paragraph 2.3.5)	Follow unused input rules for remaining receiver gate inputs if SN54S/74S140 buffer is used as line driver or Otherwise, tie all inputs of gate together if driven by other than buffer. Use SN54S/74S132 for receiver of long lines susceptible to attenuations *which* reduce signal amplitude significantly, or for added noise margins.
Flip-flops as line drivers	Not recommended, but if a flip-flop *is* used to drive an off-board load, use twisted pair cable for back-panel interconnect.
GENERAL LAYOUT RULES FOR PRINTED CIRCUIT BOARD	
Signal connections (Paragraph 2.3.4.2)	Distribute loads along direct connections where possible. Signal leads should be kept as short as possible; however, lead lengths up to 15 inches perform satisfactory in well-designed systems, especially large boards using a ground plane or ground and/or V_{CC} planes, and smaller boards using ground mesh or grid. Avoid radial fan-outs and stubs in high-frequency applications. If they are the *only* answer to driving some loads, reduce lead length proportionally and avoid sharp or abrupt bends.

Table 2.1 Guidelines for System Design Using Series 54S/74S TTL (Continued)

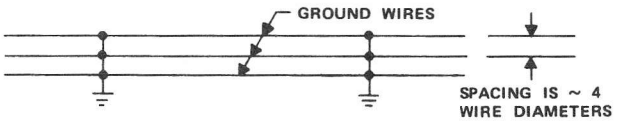
GENERAL LAYOUT RULES FOR PRINTED CIRCUIT BOARD (Continued)	
Signal connections (continued (Paragraph 2.3.4.2)	Normal on-board fan-outs and interconnections do not require terminations. Response of lines driving large numbers or highly capacitive loads can be improved with terminations of 300 ohms to V_{CC} and 600 ohms to ground in parallel with the last load if fan-out of driving output permits.
Conductor widths and spacing (Paragraph 2.3.4.2)	Signal-line widths down to 0.015-inch are adequate for most signal leads.
Signal-line spacing	Signal-lead spacing on any layer down to 0.015-inch can be used especially if care is taken to avoid adjacent use of maximum length and minimum spacing. Increase spacing wherever layout permits, paying particular attention to clock and/or other sensitive signals.
Insulator material (Paragraph 2.3.4.2)	Thickness of insulation material used for multilayer boards is not critical. If ground and V_{CC} planes or meshes are used, their capacitive proximity can be used to reduce the number of decoupling capacitors needed and this also supplements the supply bypass capacitor.
GENERAL	
Power supply (Paragraph 2.1, 2.2)	Maintain combined regulation and ripple $\leq$ 5% for Series 74S, $\leq$ 10% for Series 54S. R-F bypass supply primary.
V_{CC} Decoupling (Paragraph 2.3.3)	Decouple every 2 to 5 packages with r-f capacitors of 0.01 to 0.1 μF. Capacitors should be located as near as possible to the decoupled devices. Decouple line driving/receiving devices separately with 0.1 μF capacitors between the V_{CC} and ground pins.
On-board Grounding (Paragraphs 2.3.3, 2.3.4.2)	A ground plane is essential when the printed circuit board is relatively large (over 12 inches). Smaller boards work well with ground and/or V_{CC} mesh or grid.
System Grounding (Paragraphs 2.3.3, 2.3.4.1, 2.3.4.2)	Should as far as practicable simulate bus bars with width (W) to thickness (T) ratios (W/T) $\geq$ 4. This is normally accomplished by multiple parallel wires, or by using flat braid. If copper bus (or especially silvered-copper bus) is used, performance will be enhanced.  The W/T required will vary between systems, but a W/T $\geq$ 4 will satisfy most systems.
GATES	
Data input rise and fall times. (Paragraphs 1.5.2, 2.3.5)	Reduce as driver output impedance increases. Should be equal to or less than 50 ns/V and essentially free of ripple noise. Use SN54S/74S132 to interface with slow rising/falling or marginal input signals.
Unused input of AND and NAND gates and unused preset and clear inputs of flip-flops. (See current TI TTL Data Book)	Tie directly to +V_{CC} if interemitter voltage rating of 5.5 V maximum is not exceeded. or Tie to V_{CC} through resistor $\geq$ 1K ohms. Several unused inputs can be tied to one resistor; or Tie to used input of same gate if maximum fan-out of driving device will not be exceeded (*only high-level loading of driver is increased*); or Tie to unused gate output where unused gate input is wired to cause the unused output to remain high. Interemitter voltage should not exceed 5.5 V.

Table 2.1 Guidelines for System Design Using Series 54S/74S TTL (Concluded)

Unused inputs of NOR gates.	Tie to used input of same gate if maximum fan-out of driving device will not be exceeded; or Tie to ground
Unused gates.	Tie inputs of unused NAND and NOR gates to ground for lowest power drain. Tie inputs of unused AND gates high and use output for driving unused AND/NAND gate inputs.
Increasing gate/buffer fan-out	Parallel gates of same package. This does not include buffers such as SN54S/74S140.
FLIP-FLOPS	
Clock Pulse (Paragraphs 1.5.1, 1.5.2, 1.5.6, 1.5.7)	Drive clock inputs with STTL output whenever possible. If impossible to do, rise and fall times should be less than 50 ns/V and free of ripple noise spikes. Interface marginal digital signals with Schmitt-trigger (SN54S/74S132).

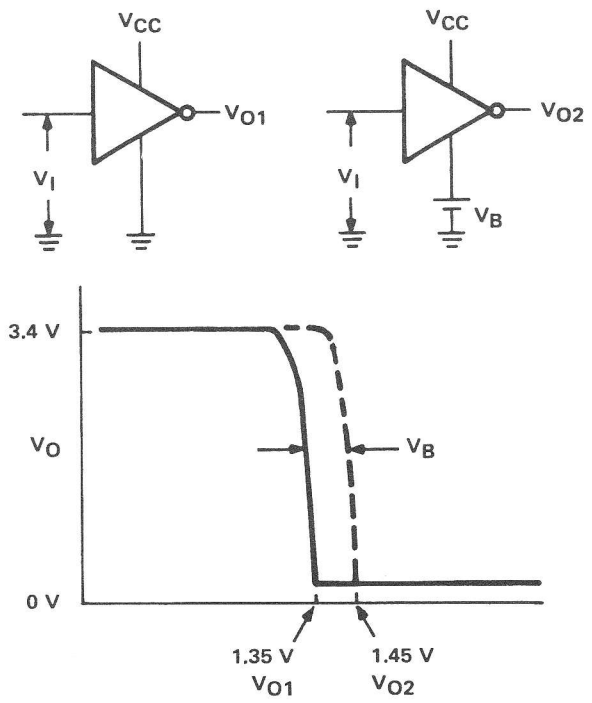


FIGURE 2.1. Effect of D-C Ground Levels on Apparent Input Levels

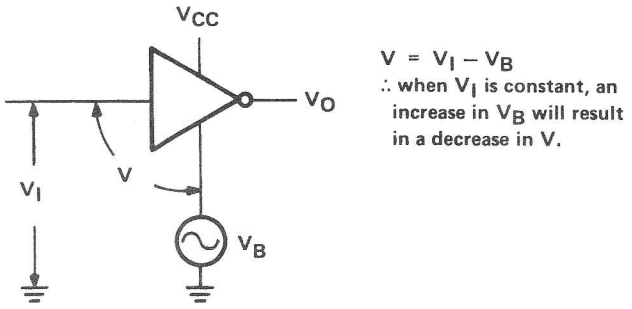


FIGURE 2.2. Effect of D-C Ground Noise on Noise Margin

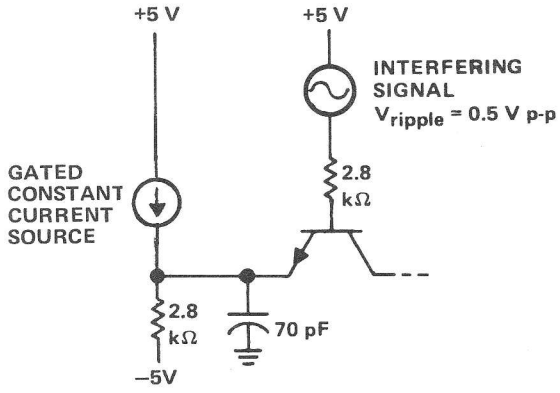


FIGURE 2.3. Effect of Input Impedance on Input Noise

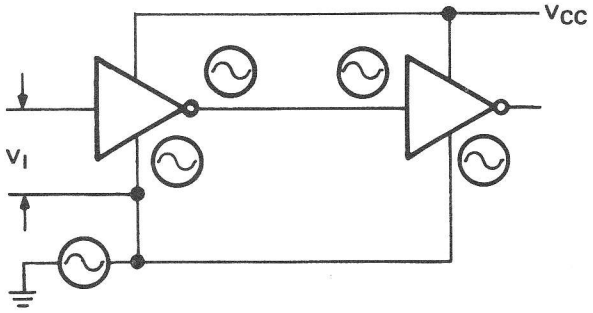


FIGURE 2.4. Low-Frequency Ripple Effects

Figure 2.5(a) is a typical digital logic circuit. The effects of noise coupled into the circuit can be seen in Figure 2.5(b) and 2.5(c) In Figure 2.5(b), a small noise pulse is present on the clock line, but the flip-flop does not respond as it does to the greater pulse in Figure 2.5(c).

If this circuit were part of some decision-making system, the condition in Figure 2.5(c) would produce erroneous answers, usually worse than no answer at all. The noise present in Figure 2.5(b), while undesirable, is not really harmful.

The origins and characteristics of such noise are considered, along with pertinent device characteristics.

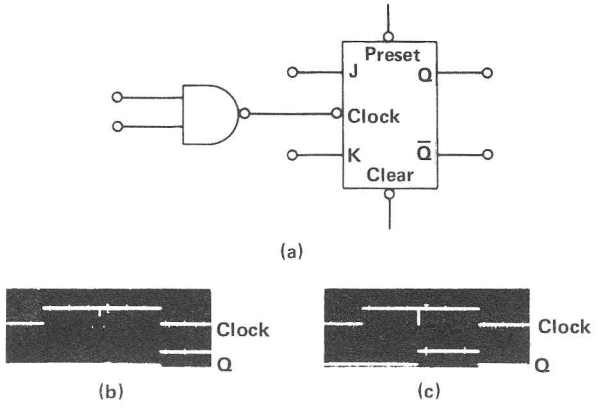


FIGURE 2.5 Typical Logic Circuit with Noisy Inputs

Methods for eliminating or counteracting the effects of noise in logic systems are presented.

2.3.1 NOISE TYPES AND CONTROL METHODS

Several types of noise must be dealt with in logic systems. The following classifications of noise are used:

a) External noise – environmental noise radiated into the system. Such noise results from circuit breakers, brush motors, arching relay contacts, or magnetic-field-generating activity.

b) Power-line noise – noise coupled through the a-c or d-c power distribution system. Initial sources are frequently the same as those of external noise.

c) Cross talk – noise induced into signal lines from adjacent signal lines.

d) Signal-current noise – noise generated in stray impedances throughout the circuit from the flow of required signal currents.

e) Transmission-line reflections – noise from unterminated transmission lines that cause ringing and overshoot.

f) I_{CC} current spikes – noise caused by synchronously switching a number of digital loads.

In general, these noise categories may be dealt with according to the following:

Noise Types	Considerations
External, Power line, Cross talk, Signal current	Shielding, Grounding, Decoupling
Transmission line, I_{CC} spikes	System properties

2.3.2 SHIELDING

Electrical equipment must function in an extremely noisy environment in addition to its own internally generated noise. Noise pulses may come from many sources, but will be an electrostatic field, electromagnetic field, or both. The noise wavefront must be prevented from entering the equipment. These noise fields are usually changing at a rapid rate; thus, the shield required to exclude them may be quite small. For effective exclusion, the sensitive circuitry must be completely shielded. Although aluminum or similar material may be effective in stopping electrostatic noise, only a ferrous metal can successfully protect equipment against magnetic fields. It is helpful to connect the system to a good earth ground, but the shield system must be complete and must be grounded to the system ground; otherwise the shield may couple the noise into the system.

External noise may be conducted into the system by the power lines. Decoupling and filtering of these lines should be standard design procedure.

2.3.3 GROUNDING AND DECOUPLING

In the generation of internal noise, the total propagation delay is of secondary importance. It is the actual transition time that determines the amplitude/frequency spectrum of the generated signal at the higher harmonics. Application of the Fourier integral to Series 54S/74S waveforms shows frequency components of significant amplitude exceeding 100 megahertz. In consideration of the frequency spectrum generated when a Series 54S/74s device switches, it is obvious that a system using these devices must receive consideration from an RF viewpoint if trouble is to be avoided, even though the repetition rates may be only a few megahertz. The transient currents generated by charging capacitance, changes in levels of direct current, line driving, etc., must be considered. For example, a gate driving a transmission line may be represented by a voltage source E having an output impedance Z_S connected to an impedance Z_0, and loaded with resistance R (Figure 2.6).

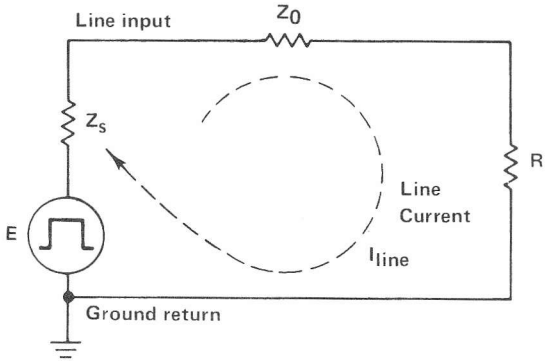


FIGURE 2.6 Simplified Circuit of a Gate Driving a Loaded Transmission Line

Line termination is not a factor in drive current until after a reflected pulse returns from the termination to the transmitting device.[2] In a practical TTL circuit, the line termination must be high relative to the Z_0 of the line. Assume the voltage E is 5 volts in amplitude, the Z_S of the source is 50 ohms and the Z_0 of the line is also 50 ohms. When E makes the transition from 0 volt to 5 volts, the

voltage across the input of the line will be, by Ohm's law.

$$V_{in} = E \frac{Z_0}{V_s + Z_0} = 2.5 \text{ V}$$

Now for the 50-ohm line to become charged, a current must flow onto the line equal to

$$I_{line} = \frac{V_s}{Z_0} \quad \frac{2.5}{50} = 50 \text{ mA}$$

This current also flows in the ground return, in this case the transmission-line ground. If the line and return are originated and terminated close to the driving and receiving devices, there is no discontinuity in the line. Where the ground is poorly returned, the currents flowing see the discontinuity in the cable as a high impedance, and a noise spike is generated. Viewed in a slightly different manner, the ground current sees a low impedance and a current cancellation if the ground is properly carried through; if not, it sees a high impedance. See Figure 2.7 for a specific

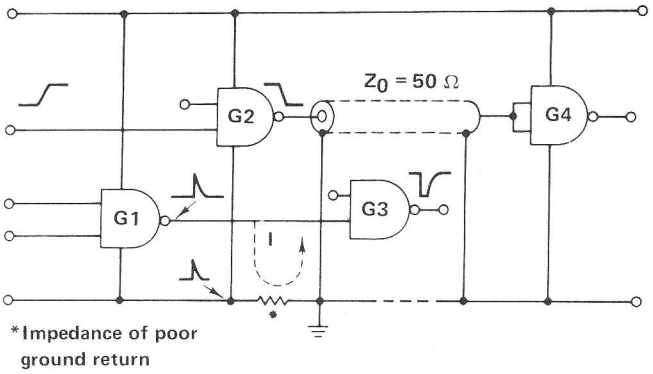


FIGURE 2.7 Noise Generation Due to Poor Transmission Line Returns

example. Assume the gate driving the line is switched from the 1 to the 0 state. Current flows is indicated by the arrow marked I. Since the line is improperly returned to the driver, a pulse is developed across the impedance. A possible consequence is the false output of gate 3 (G3).

If the ground return is properly made, desirable results are obtained. The impedance discontinuity is eliminated and current cancellation occurs at the ground point. Undesirable voltage spikes are then eliminated. Two rules to reduce transmission-line currents to acceptable levels in TTL systems may be established. These are empirical rules found to be effective (see Figures 2.8 and 2.9).

a) Carry all returns, including twisted pair and coaxial cables, to a good ground termination and ground line returns close to the driving and receiving devices. Figure 2.8 illustrates the necessity for this practice.

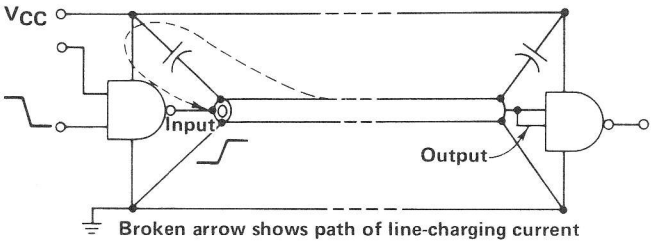


FIGURE 2.8 Ideal Transmission-Line Current Handling

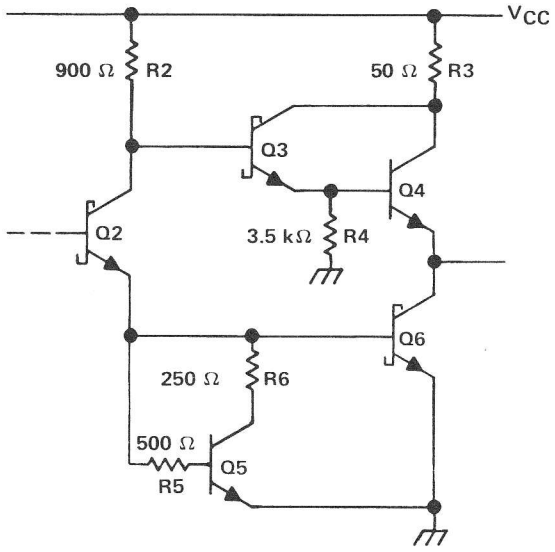


FIGURE 2.9 STTL Totem-Pole Output Stage

b) Decouple V_{CC} of line-driving and line-receiving gates close to the device with a 0.1-microfarad disk ceramic capacitor.

As the logic devices change state, current levels change because of different device currents required in each state, to external loading, to transients caused by charging and discharging capacitive loads, and to conduction overlap in the totem-pole output stage. When a gate changes states, its internal current changes from I_{CCH} to I_{CCL} (these values are stated on the data sheet for each device). Also any capacitance, stray or otherwise, must be charged or discharged for a logic state change. The capacitance must be charged by a current:

$$I_C = \frac{dv}{dt}$$

If we know the total stray capacitance on a gate output, the logic level voltage excursion, and associated rise or fall times, then the ideal-case instantaneous current during the transition can be calculated.

From this equation, it can be seen that the current transient for charging load capacitance will increase with the higher speed TTL circuits. Therefore, the Series 54LS/74LS circuits will have lower transient current than the Series 54S/74S circuits. Another parameter that should

be considered is the value of R3 (Figure 2.9). Resistor R3 acts as a limit on the charging current.

The current required for charging C_L, shown in Figure 2.10, is supplied by the V_{CC} supply when the transition is from logical 0 to logical 1 at the output of G1.

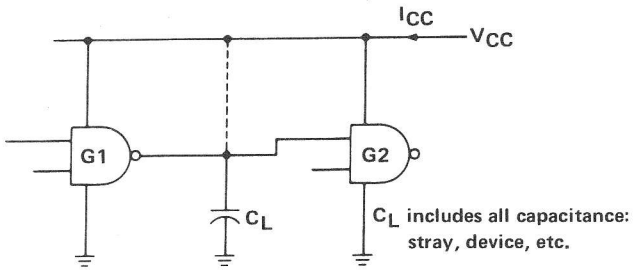


FIGURE 2.10 Circuit Showing Effective Capacitive Loading

When the output of G1 goes from logical 1 to 0, the capacitance C_L is shorted to ground by transistor Q6 (Figure 2.9) and so has no effect on I_{CC}.

A characteristic common to all TTL totem-pole output stages contributes an additional current transient when the output changes from a logical 0 to a 1. This transient, or spike, is caused by the overlap in conduction of the output transistors Q4 and Q6 of Figure 2.9. The situation arises because Q4 can turn on faster than Q6 can turn off. This allows a direct circuit for the supply voltage to ground which is limited by R_{CS} of Q4, Q6, and R3. For all Series 54/74 TTL circuits except Series 54S/74S circuits, the peak current can be estimated by

$$I_{CC(max)} = \frac{V_{CC} - V_D - 2V_{CEsat}}{R_{(output\ collector)}}$$

The total charge that flows because of conduction overlap is determined by the equation above and the duration of the overlap. As would be expected, the low-power TTL series has the lowest current spikes and the longest duration because of the slower speeds. Conversely, Series 54H/74H TTL exhibits higher current spikes of shorter duration.

The total I_{CC} switching transient is then a combination of these three major effects: 1) difference in I_{CCH} and I_{CCL}, 2) the charging of load capacitance, and 3) conduction overlap. Tests were made to show these effects, and the results are given in Figure 2.11. First, four types of Series 54/74 were tested with no load (the scope probe was connected to the output only when measuring V_{out}, and the photos were double-exposed). This was intended to approximate the effects of conduction overlap isolated from the transient caused by charging load capacitance. Notice that different scales are used in several of the comparisons. The results are almost as predicted: the SN74L00 has the lowest transient, and the SN74H00 has the highest. But the SN74S00 should be higher, since it is the fastest circuit. The reason for the decrease can be explained by referring to Figure 2.9. The additional transistor Q5 and associated resistors give more closely matched switching times for the output transistors Q4 and Q6, resulting in a smaller transient even though the typical rise time is 3 nanoseconds compared to 9 nanoseconds for the Series 54/74.

The second series of tests (Figure 2.11) covers a capacitive load of 50 picofarads. For this test, all the I_{CC} transient peaks increase in amplitude and width. It is interesting to note, in comparing the Series 74S and Series 74H, that the transients for the two are more nearly equal, because the part of the transient resulting from the added C_L now predominates over the contribution made by the conduction overlap effect. Voltage spikes on V_{CC}, measured at the IC package, are also increased, because of the larger transient currents.

From these tests, one can conclude that the condition to be avoided (the only one that can be avoided) is unnecessary stray capacitance in circuit wiring. The charging of load capacitance, in most cases, overshadows the other two effects with respect to noise produced on the V_{CC} line by switching current transients.

The flow paths of these currents have been investigated to determine the grounding and decoupling necessary to counteract their effects. V_{CC} decoupling may be approached in two ways: common to both is the requirement to maintain low impedance from the individual circuit V_{CC} to ground. First, the V_{CC} line may be considered a transmission line back to a low impedance supply. The positive bus may be laminated with a ground bus to form a strip transmission line of extremely low impedance (see paragraph 2.3.4.2). Such a line may be electrically approximated with lumped capacitances (Figure 2.12). The inductances are usually a distributed component which must be minimized to lower the Z_0 of the line. An alternative approach is to consider the V_{CC} bus as a d-c connecting element only and provide a low-impedance path near the devices for the transient currents to ground (Figure 2.13). For effective filtering and decoupling, the capacitors must be able to supply the change in current for a period of time greater than the pulse width of this current. Since the problem is one of essentially d-c changes due to logic state changes, coupled with high frequency transients associated with the changes, two different values of time constant must be considered. Capacitors combining the high capacitance required for long periods with the low series reactance required for fast transients are prohibitive in cost and size. A good compromise is the arrangement shown in Figure 2.14. Typical component values may be found for the r-f capacitor C2, assuming the parameters have common values such as:

$$\Delta I_{CC} = 50\ mA$$
$$\Delta V \leqslant 0.1\ V$$
$$\Delta T = 20\ ns$$

then

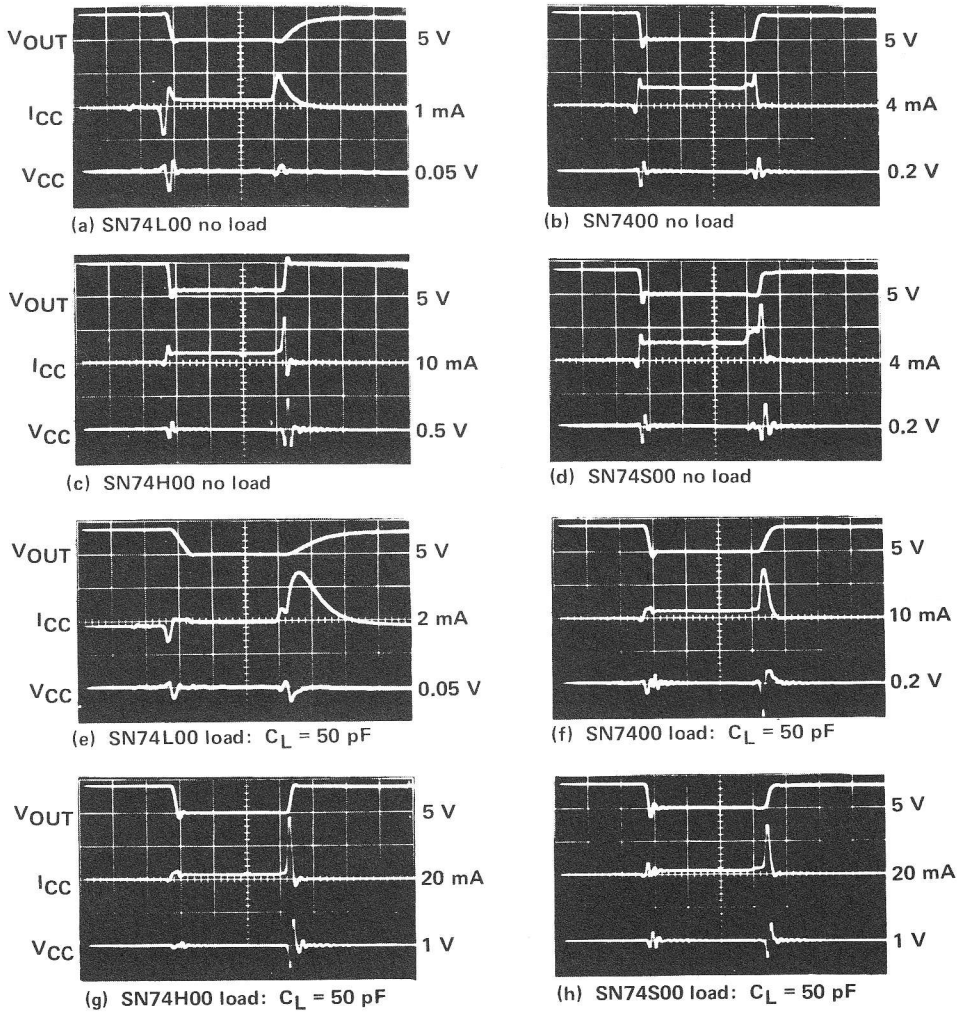
$$C2 = \frac{\Delta I_{CC}}{\Delta V/\Delta T} = \frac{50 \times 10^{-3}}{0.1/(20 \times 10^{-9})}$$

$$= \frac{(50)(20) \times 10^{-12}}{0.1}$$

$$= 10{,}000 \times 10^{-12}$$

$$= 0.01\ \mu F$$

The same approach may be used for the low-frequency capacitor C1. However, the factor ΔT, which was merely a worst-case transient time when calculating C1, now becomes a bit hazy. An analysis of the current cycling on a statistical basis is the best approach in all but the simplest systems. The recommended procedure is to decouple with 10 microfarads to 50 microfarads.



1. V_{CC} = 5 V
2. Sweep is 50 ns/division
3. Rise and fall times of input pulse are 10 ns
4. Vertical scales are in units shown per division

FIGURE 2.11 I_{CC} Transient, Comparing TTL Types

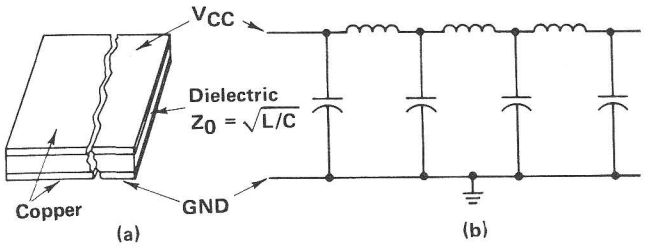


FIGURE 2.12 Transmission-Line Power Buses

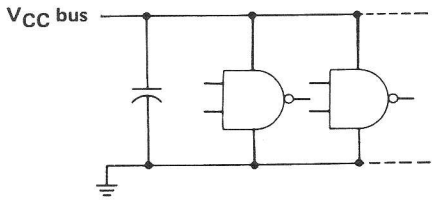


FIGURE 2.13 Capacitive Storage V_{CC} System

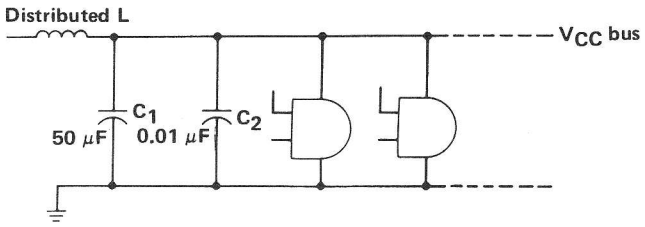


FIGURE 2.14 Commonly Used Power Distribution and Decoupling System

A discrete inductance of 2 microhenries to 10 microhenries is sometimes added for further decoupling. However, its benefits are questionable, and its usefulness should be evaluated for the individual system. The low-pass filter formed must be capable of keeping the transients confined and off the distribution bus. The possibility of resonance in the inductor or LC combination must be considered.

Noise spikes on the V_{CC} line that do not force the gate output below the threshold level are not serious. Downward spikes as great as 3 volts have been tolerated on the V_{CC} line without propagating through the logic system. Thus, the system designer can be greatly relieved on the subject of V_{CC} noise if even minimal consideration is given to the subject.

Ground noise is another matter. Pulses on a high-impedance ground line can quite readily exceed the noise threshold. Only if a good ground system is maintained can this problem be overcome. If proper attention is paid to the ground system, problems seldom arise.

The concept of a common ground plane structure as used in r-f and high-speed digital systems is quite different from that of the common ground point as used in low-frequency circuits. The more closely the chassis and ground can approach being an integral unit, the better the noise suppression characteristics of the system. Consequently, all parts of the chassis and ground bus system should be bound tightly together electrically and mechanically. Floating or poorly grounded sections not only break the integrity of the ground system, but may actually act as a noise distribution system.

The matter of grounds and decoupling on printed boards requires some attention. The most desirable arrangement would be a double-clad or multilayer board with a solid ground plane or mesh. Where component density prohibits this, the ideal should be relaxed only as far as necessary. Cross talk and ground noise can best be reduced on large boards with a ground plane. Some suggestions for board grounds where a plane is not practical are:

a) Make the ground strap as wide as possible everywhere, even though this may mean its width varies radically.

b) Form a complete loop around the board; bring both sides of the board through separate pins to the system ground.

The V_{CC} line can provide part of the ground mesh on the board, provided it is properly decoupled. For a TTL system, a good rule of thumb is 0.01 microfarad per synchronously driven gate and at least 0.1 microfarad per 20 gates, regardless of synchronization. This capacitance may be lumped, but it is more effective if distributed over the board. A good rule to follow is to permit no more than 5 inches of wire between any two package V_{CC} points. R-f-type capacitors for decoupling are mandatory; disk ceramics are a good choice. It is sometimes a good practice to decouple the board from the external V_{CC} line with a 2.2-microfarad capacitor as stated earlier, but this is optional, and the r-f capacitors will still be required. In addition, it is strongly recommended that gates driving long lines have the V_{CC} supply decoupled at the gate V_{CC} terminal and that the capacitor ground, device ground, and transmission-line ground be brought to a common point. The reasons for this should be more obvious after studying the currents involved in switching and line driving.

2.3.4 CROSS TALK

When currents and voltages are impressed on a connecting line in a system, it is impossible for adjacent lines to remain unaffected. Static and magnetic fields interact and opposing ground currents flow, creating linking magnetic fields. These cross-coupling effects are lumped together as cross talk.

2.3.4.1 Back-Panel Interconnections

Interconnecting signal lines can be grouped into three broad categories: coaxial lines, twisted-pair lines, and straight wire lines. Because of the low impedance and shielding characteristics of coaxial cable, coaxial cable cross talk is minimal and is no problem with TTL.

Figure 2.15 is descriptive of practical types of signal transmission lines. The mutual reactances L_m and C_m, which form the noise coupling paths, and the line parameters L_s and C_g, which govern the Z_0 of the line, will vary with the type of line used. Since cross talk is a function of the ratio of the mutual impedances to the line characteristic impedances, the selection of transmission-line type must be at least partially a factor in cross talk considerations.

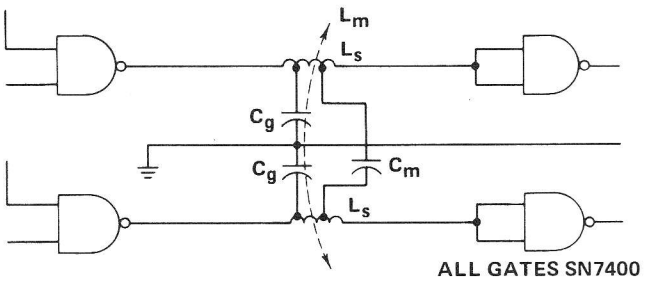


FIGURE 2.15 Equivalent Circuit for Sending Line

Direct-wired connections are the simplest and cheapest approach, but they are also the poorest for noise rejection. It is possible to use direct leads up to 12 inches in length, if the lead is not cabled tightly together with similar leads.

When the length of the signal line increases, the line impedance is seen by the driving and receiving gates. As shown in Figure 2.16, a pulse sent along the sending line

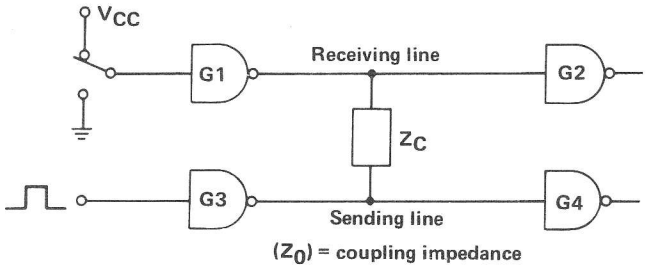


FIGURE 2.16 Coupling Impedances Involved in Cross Talk

G3-G4 will be coupled via coupling impedance Z_c onto the receiving line G1-G2, which can be in either of the two logic states. The extent to which cross talk will occur depends on the type of lines used and their relationship to each other.

The voltage impressed on line G3-G4 by gate G3 is

$$V_{SL} = \frac{V_{G3}Z_0}{R_{S3} + Z_0}$$

where

V_{G3} = open-circuit logic voltage swing generated by gate G3

R_{S3} = output impedance of G3

Z_0 = line impedance

V_{SL} = voltage impressed on the sending line

The relationship for the above equation is illustrated in Figures 2.17 and 2.18.

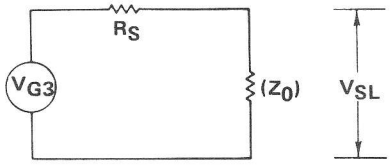


FIGURE 2.17 Capacitive Cross Talk Between Two Signal Lines

The coupling from the sending line to the receiving line can be represented by taking the coupling impedance Z_c into account. An equivalent circuit to represent the coupling from the sending line to the receiving line is shown in Figure 2.18.

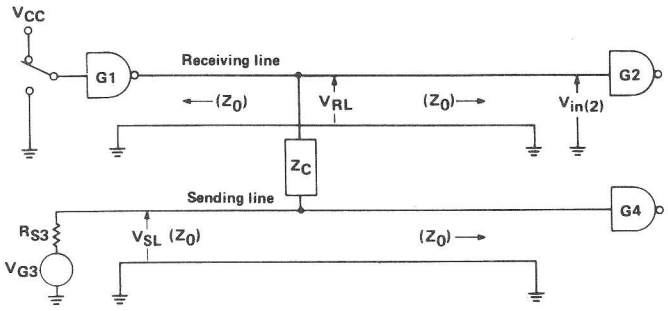


FIGURE 2.18 Equivalent Circuit for Cross Talk

Two Z_0 loads are shown at the receiving line to represent the fact that, from the theoretical lumped coupling point in the receiving line, there are two lines in parallel, one going to gate G1 and one to gate G2. The voltage V_{RL} developed across the receiving line is therefore

$$V_{RL} = V_{SL} \frac{Z_0}{2(Z_c + Z_0)}$$

Since the input impedance of gate G2 will almost invariably be large compared with Z_0, the full open-circuit output voltage of the receiving line will appear at the input of G2. Therefore,

$$V_{in(2)} = 2\,V_{RL}$$

Thus

$$\frac{V_{in(2)}}{V_{G3}} = \frac{Z_0 \times Z_0}{(Z_c + Z_0)(R_{S3} + Z_0)}$$

If $R_{S3} \ll Z_0$, this expression may be simplified to

$$\frac{V_{in(2)}}{V_{G3}} = \frac{1}{1 + Z_c/Z_0}$$

which will be the cross talk noise-to-signal ratio of this transmission system.

The worst case for signal-line cross talk occurs when sending and receiving lines are close together but widely separated from a ground return path. The lines then have a high characteristic impedance and a low coupling impedance Z_c. For example, if the lines consist of 1/25-inch conductors spaced 1/30 inch apart and farther then 0.78 inch from any ground conductors, the impedances will be $Z_0 \approx 200$ ohms and $Z_M \approx 80$ ohms. The signal-to-noise ratio will then be

$$\frac{V_{in(2)}}{V_{G3}} = \frac{1}{1 + 80/200} = 0.71\,V$$

This is clearly unsatisfactory, for currently no very high-speed logic circuit has a guaranteed noise margin greater than one-third the logic swing. Such potential cross talk can be avoided by preventing such close spacing of conductors.

If, in this example, a ground plane were introduced, spaced 1/25 inch from each conductor, the impedances become $Z_0 \approx 50$ ohms and $Z_c \approx 125$ ohms. Substituting these values yields

$$\frac{V_{in(2)}}{V_{G3}} = \frac{1}{1 + 125/50} = 0.29\ V$$

Although this degree of cross talk would probably not be disastrous in a Schottky TTL system, it does reduce the guaranteed d-c noise margin.

If the sending and receiving lines were twisted pairs laid closely side by side, the impedances would be $Z_0 \approx$ 80 ohms and $Z_c \approx 400$ ohms. The cross talk noise-to-signal ratio would then be

$$\frac{V_{in(2)}}{V_{G3}} = \frac{1}{1 + 400/80} = 0.17\ V$$

This is safe and practical for all conventional logic circuits including Series 54S/74S TTL.

Mutual coupling can be reduced by using coaxial cable or shielded twisted pairs. When mutual inductance and capacitance are decreased, however, line capacitance is increased, imposing restrictions on the driver. Coaxial cable combines very high mutual impedance with low characteristic impedance, and shielding as well. It effectively eliminates cross talk, but it is necessary in only the noisiest environments. Twisted pairs are usually adequate, and are typically less expensive and easier to use.

2.3.4.2 Printed Circuit Card Conductors

Signal interconnections on a two-sided or multilayer printed circuit card can be grouped into two general categories: microstrip lines and strip lines. As illustrated in Figure 2.19, the microstrip line consists of a signal conductor separated from a ground plane by a dielectric insulating material.

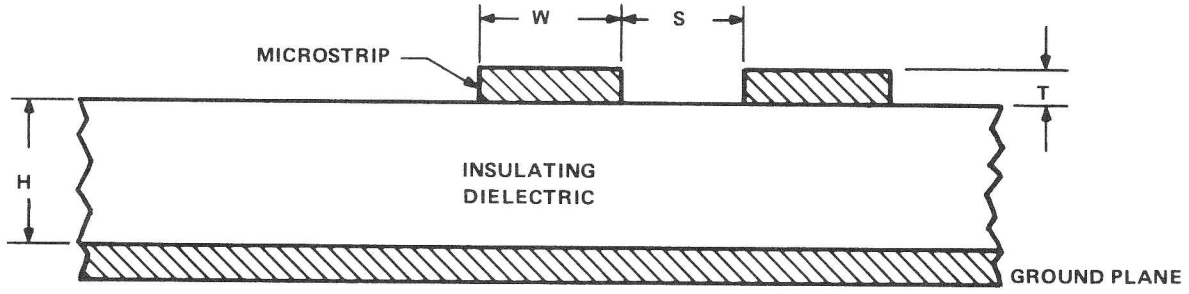


FIGURE 2.19 Microstrip Line

A strip line, illustrated in Figure 2.20, consists of a signal conductor within a dielectric insulating material and the conductor being centered between two parallel conductor planes.

The important features of these type printed circuit conductors are that the impedances are highly predictable, can be closely controlled, and the process is relatively inexpensive as standard printed circuit board manufacturing techniques are used. Typical impedances of these types of conductors with respect to their physical size and relative spacings are shown in Tables 2.2 and 2.3.

Cross talk on the printed circuit board is also a function of the mutual reactances and the line parameters which govern the Z_0 of the line. A microstrip line and a strip line are, by definition, conductors placed relatively close to a ground plane; thus, they have at least one inherent property which tends to reduce cross talk. In addition, the thickness (H) of the dielectric and the spacing (S) of the conductors can be implemented selectively to reduce the amount of possible cross talk. The effects of these two dimensions on cross talk have been evaluated[3] and are shown graphically in Figure 2.21. The data shown can be used to estimate the maximum cross talk which will be encountered under the most unfavorable conditions.

This occurs when a quiet line is adjacent to a signal line and the quiet line has a low impedance at the far end of the line and a high impedance at the near end. This condition is shown in Figure 2.22.

Referring to the curves for the cross talk constant of this configuration (Figure 2.21), the data point shown by a dot on the cross talk curve has the configuration shown in Figure 2.23.

The cross talk between adjacent leads separated by the distance S was found to be 30 millivolts/inch. The cross talk between the two leads separated by the distance H′ was found to be 60 millivolts/inch. The amplitude for the cross talk reached a maximum with 10 inches of adjacent length, and only the pulse duration increased with increasing line length.

Two other conditions, represented by an X on the cross talk constant curves, were evaluated on a two-sided board (Figure 2.19) having the following dimensions:

S = 30 mils
H = 60 mils

The conductor length is 16 inches, and the waveforms generated are shown in Figure 2.24. The conditions shown

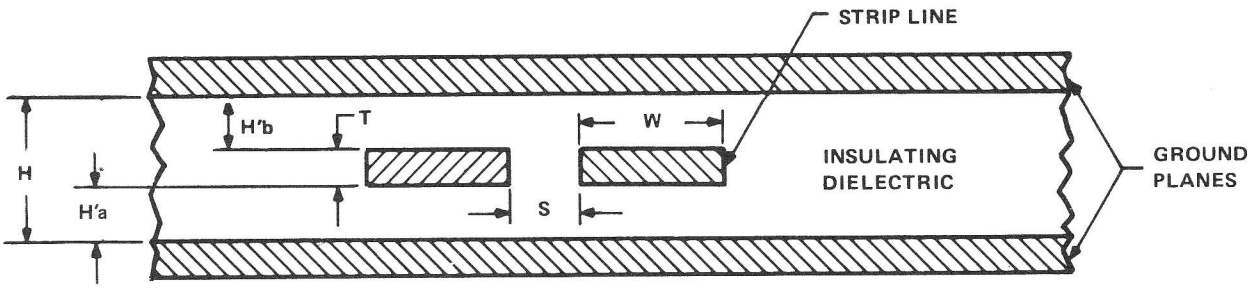


FIGURE 2.20 Strip Line

Table 2.2 – Typical Impedance of Microstrip Lines

Relative dielectric constant ≈ 5

Dimensions		Line Impedance	Capacitance
H(mils)	W (mils)	$Z_0(\Omega)$	per Foot (pF)
6	20	35	40
6	15	40	35
15	20	56	30
15	15	66	26
30	20	80	20
30	15	89	18
60	20	105	16
60	15	114	14
100	20	124	13
100	15	132	12

Table 2.3 – Typical Impedance of Strip Lines

Relative dielectric constant ≈ 5, and H'a = H'b

Dimensions		Line Impedance	Capacitance
H'a = H'b = (mils)	W (mils)	$Z_0(\Omega)$	per Foot (pF)
6	20	27	80
6	15	32	70
10	20	34	67
10	15	40	56
12	20	37	57
12	15	43	48
20	20	44	48
20	15	51	42
30	20	55	39
30	15	61	35

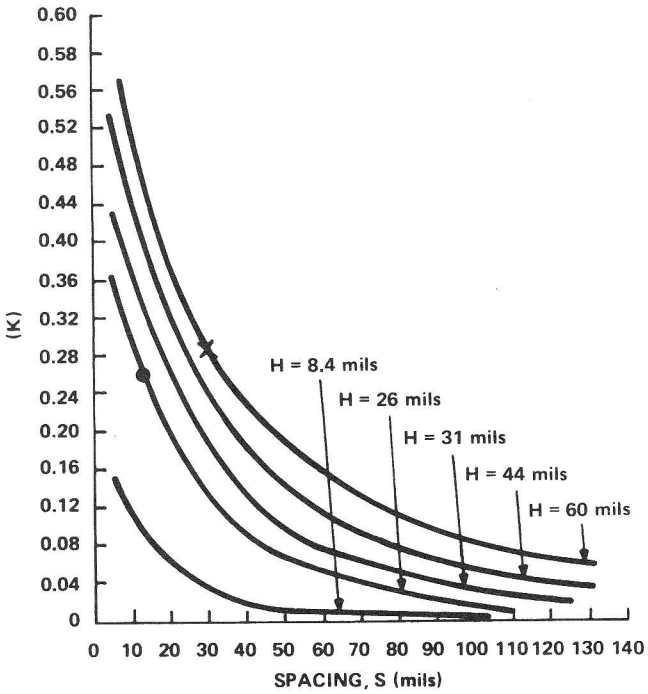


FIGURE 2.21 Line Spacing versus Cross Talk Constant

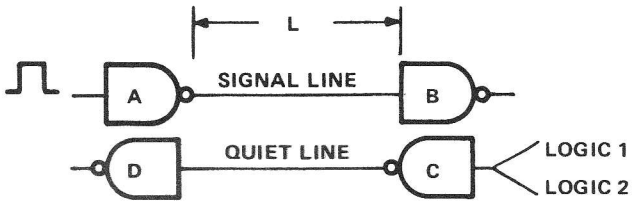
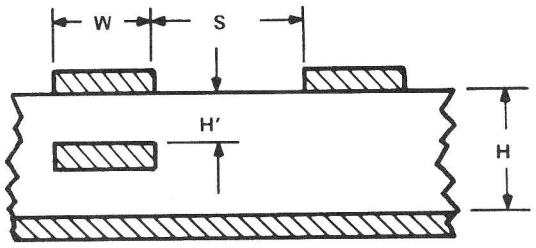


FIGURE 2.22 Cross Talk Test Circuit



S = 12 MILS
H = 25 MILS
H' = 6 MILS
W = 8 MILS

FIGURE 2.23 Dimensional Data for Cross Talk Test Circuit

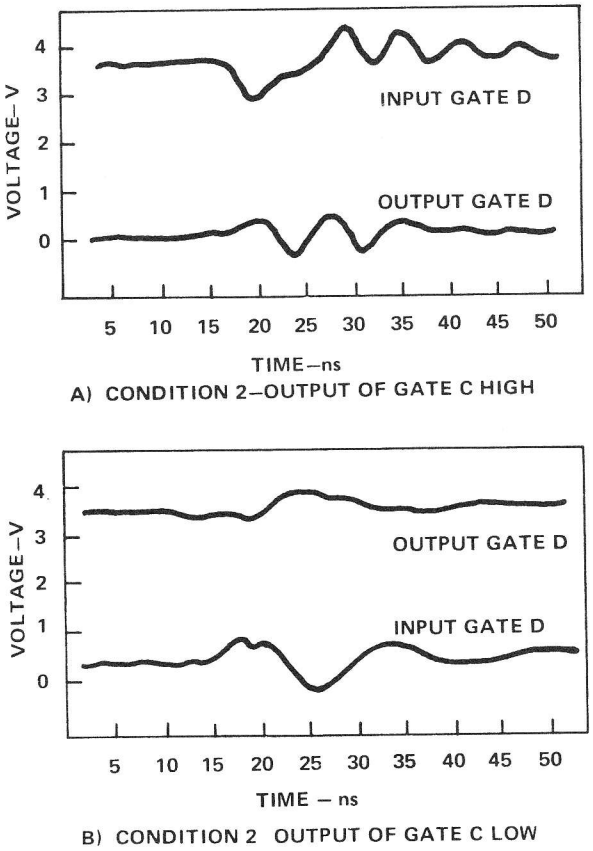


FIGURE 2.24 Voltage Waveforms of 16-Inch Conductor on Two-Sided Board

are: One with the input of gate C at a logic 0 level, and one with the input of gate C at a logic 1 level. Although the noise margins were reduced, erroneous data was not transmitted.

2.3.5 TRANSMISSION-LINE DRIVING REFLECTIONS

When the interconnections used to transfer digital information become long enough so that line propagation delay is equal to or greater than the pulse transition times, the effects of reflections must be considered. These reflections are created because most TTL interconnections are not terminated in their characteristic impedance. Reflections lead to such things as reduced noise margins, excessive delays, ringing, and overshoot. Some method must be used to analyze these reflections. Basic transmission-line equations are applicable but unwieldy, since neither the gate's input nor output impedance is linear. Transmission-line characteristics of TTL interconnections can best be analyzed by a simple graphic technique.

Figure 2.25 shows piecewise linear plots of a gate input and both (logical 0 and 1) conditions of the output for a typical Series 54S/74S device. The output curves are

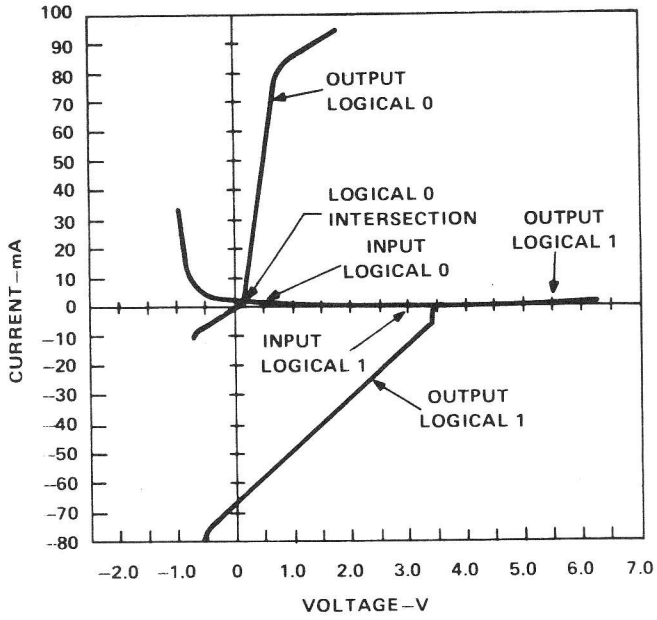


FIGURE 2.25 Series 54S/74S Bergeron Diagram

plotted in the normal way with positive slopes, but the input is inverted, since it will be at the receiving end of a transmission line. The logical 0 and 1 intersections are indicated on the plot. These points are the steady state values which will be observed on a lossless transmission, such as shown in Figure 2.26.

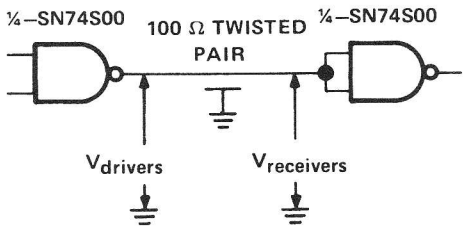


FIGURE 2.26 Series 54S/74S Driving Twisted Pair

Figure 2.26 shows a typical TTL interconnection using twisted-pair cable which will usually have characteristic impedances of about 100 ohms. To evaluate a logical 1-to-0 transition, Figure 2.27 is used. The line $-1/Z_0$ (Z_0 = 100 ohms), which represents the transmission line, is

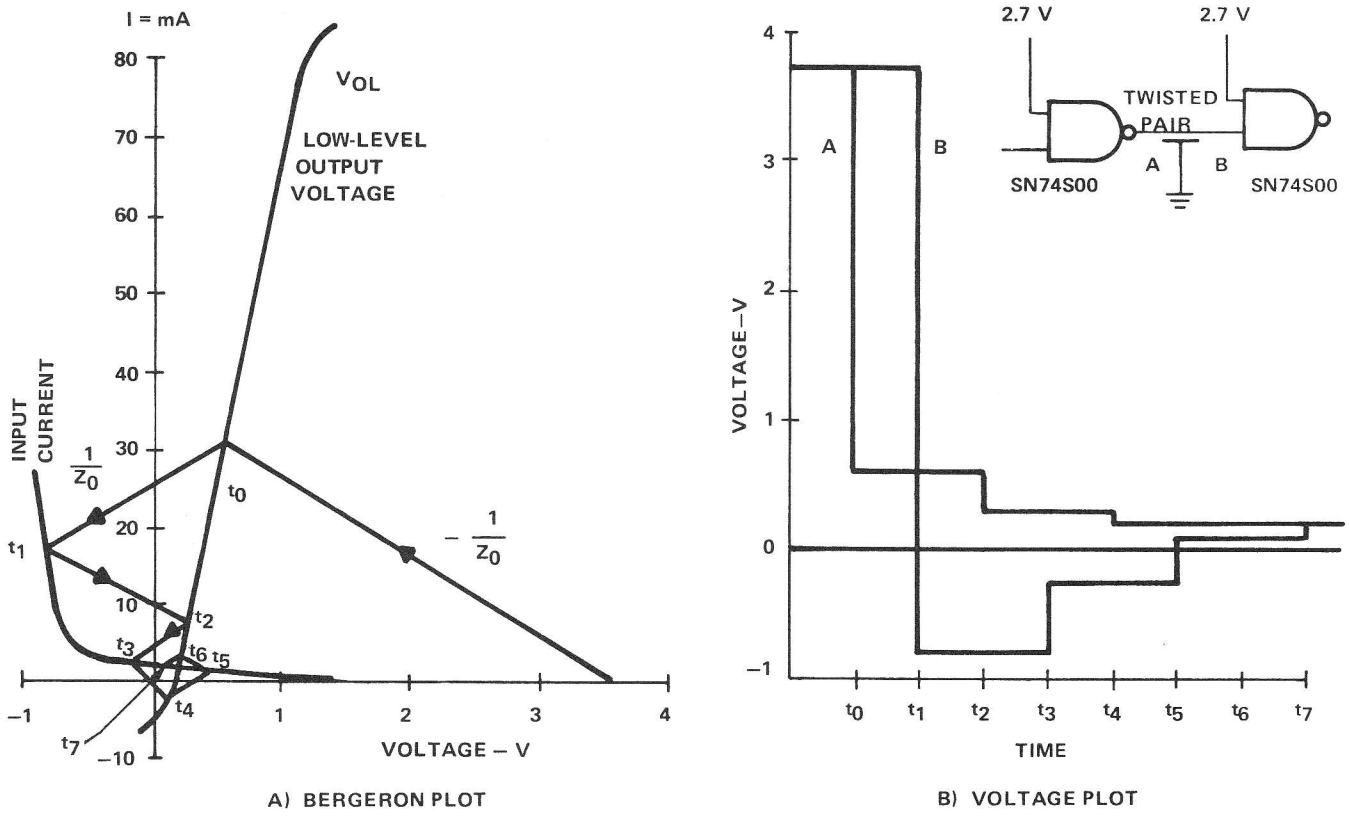


FIGURE 2.27 Negative Transition – 100-Ohm Unterminated Line

superimposed on the output characteristic curves in the Bergeron plot. Since evaluation of a logical 1-to-0 transition is desired, the $-1/Z_0$ line starts at the point of intersection of the impedance curves of the input and output for a logical 1 conditon. The slope $-1/Z_0$ then proceeds toward the logical 0 output curve. At time t_0, the driver output voltage is determined by the intersection of $-1/Z_0$ and the output 0 curve (+0.50 volt). The transmission-line slope now becomes $+1/Z_0$ and is drawn toward the input curve. At time t_1 ($t_{n+1} - t_n$ = time delay of line), the receiving gate sees −0.75 volt. Now the line slope changes back to $-1/Z_0$, and the curve continues as the intersection of the input and output curves for a logical 0 is approached. Figure 2.27 also plots driver and receiver voltages versus time in this case.

A logical 0-to-1 transition is treated in approximately the same manner (Figure 2.28). The Bergeron line $-1/Z_0$ starts at the intersection for a logical 0. At time t_0, the driver's output rises to +2.4 volts, and at time t_1, the receiving gate's input goes to about +5.0 volts. Ringing occurs on the line because both ends are terminated in a high impedance. This ringing decreases in amplitude as a steady state condition is approached. Both the output and input voltages are plotted in Figure 2.28 for this case.

In Figures 2.29 and 2.30, graphic analysis is applied to a 50-ohm transmission line. Notice that a decrease in line impedance does not significantly change the logical 1-to-0 transition characteristics. This is because of the low driver output impedance in the 0 state and the presence of an integral clamping diode on the input of the receiving gate. Line impedance does, however, significantly alter the 0-to-1 transition characteristics. As the line impedance increases, overshoot at the receiving end also increases, and low impedance lines significantly affect noise margins of gate inputs placed near the driver. Unusually high impedance lines, especially long lines, can be pulled up with a medium-value resistor (300 to 600 ohms) to improve noise margin and rise times.

The scope photographs in Figures 2.31 through 2.34 were taken to show the effectiveness of the graphic techniques. In most cases, the calculated and experimental values of voltage steps agree within reason. The ringing that appears for the open wire is not immediately obvious, but this is because the input and output curves in this region lie practically along the positive horizontal axis. At the scale used for the graphic analysis, it is difficult to go much beyond the first few reflections. As stated before, the graphic analysis is idealized; stray capacitance and inductance are not considered.[3,4] Voltage waveforms of a Schottky gate driving a 50-ohm coaxial cable and a 100-ohm twisted pair cable are shown in Figure 2.35.

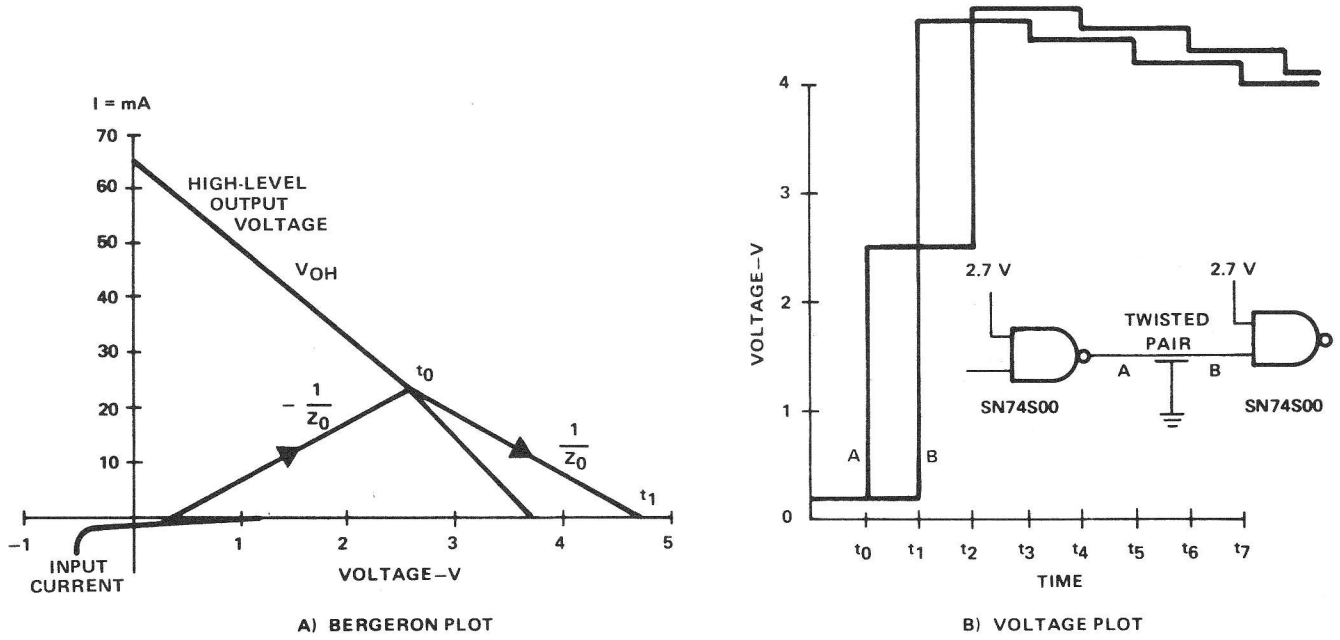


FIGURE 2.28 Positive Transition – 100-Ohm Unterminated Line

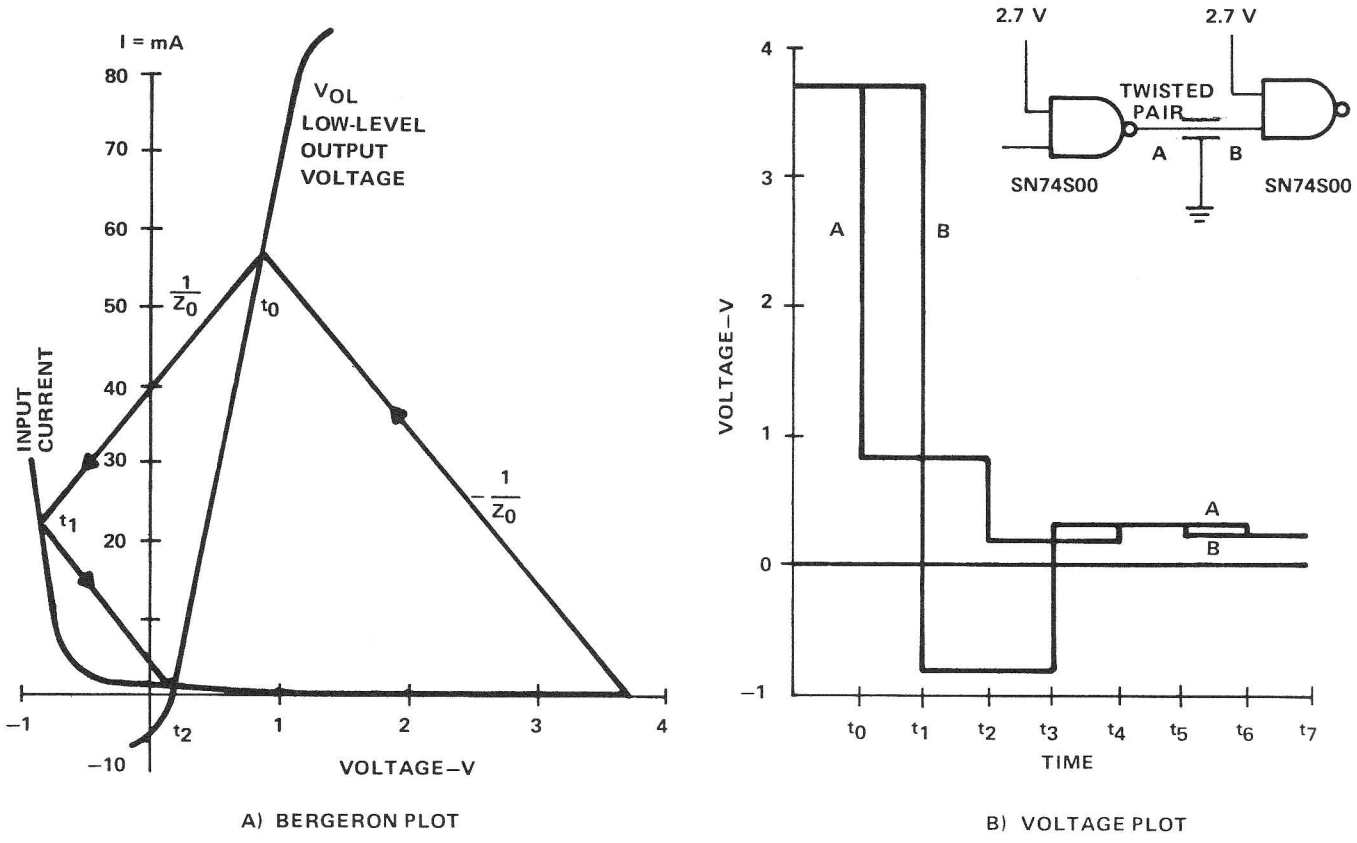


FIGURE 2.29 Negative Transition – 50-Ohm Unterminated Line

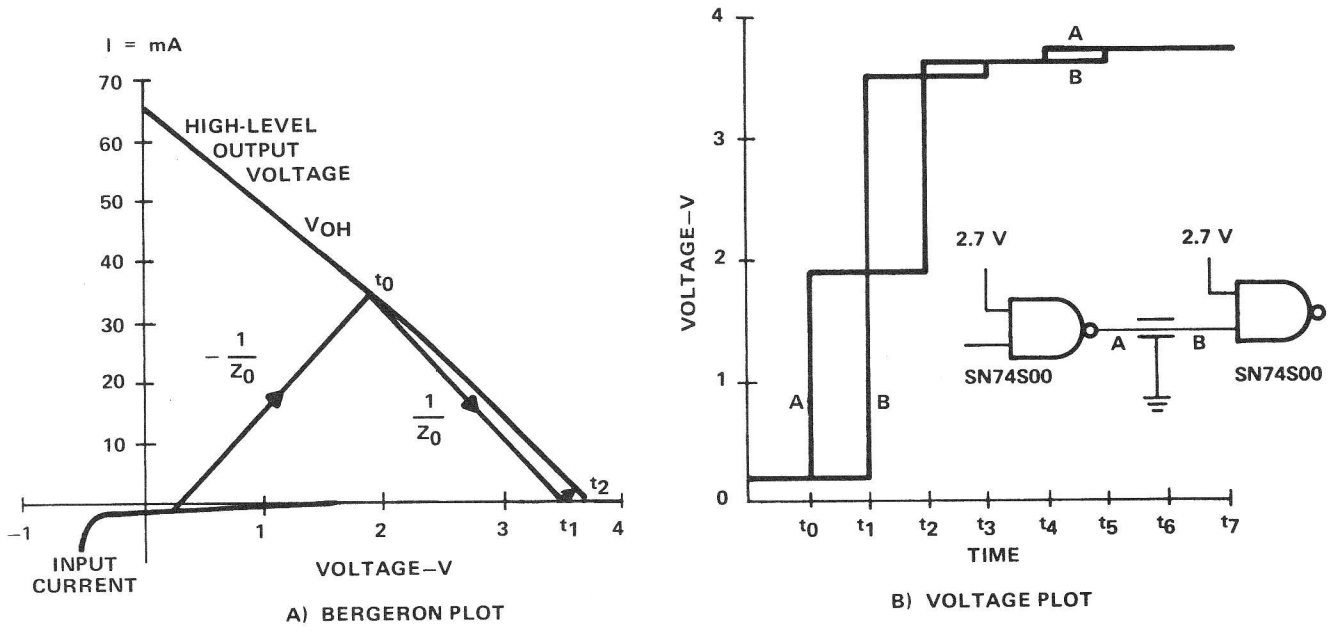
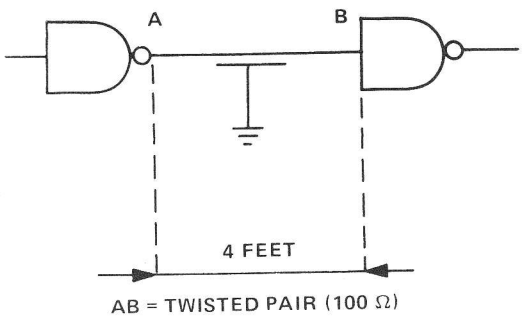
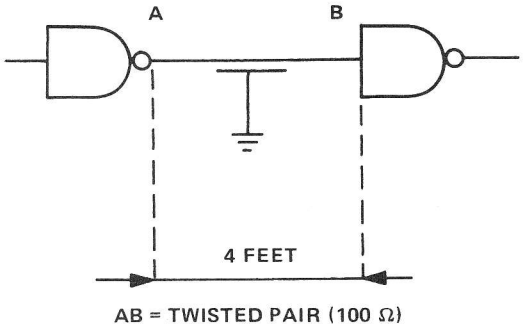


FIGURE 2.30 Positive Transition – 50-Ohm Unterminated Line





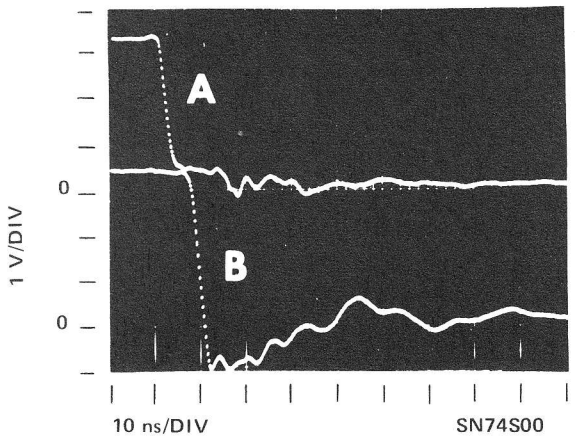


FIGURE 2.31 Negative Transition – 100-Ohm Unterminated Line

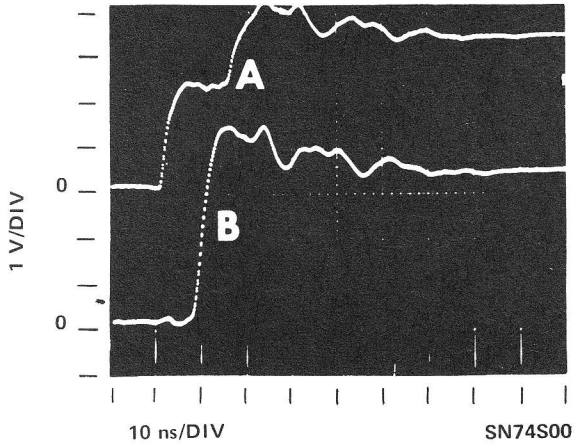


FIGURE 2.32 Positive Transition – 100-Ohm Unterminated Line

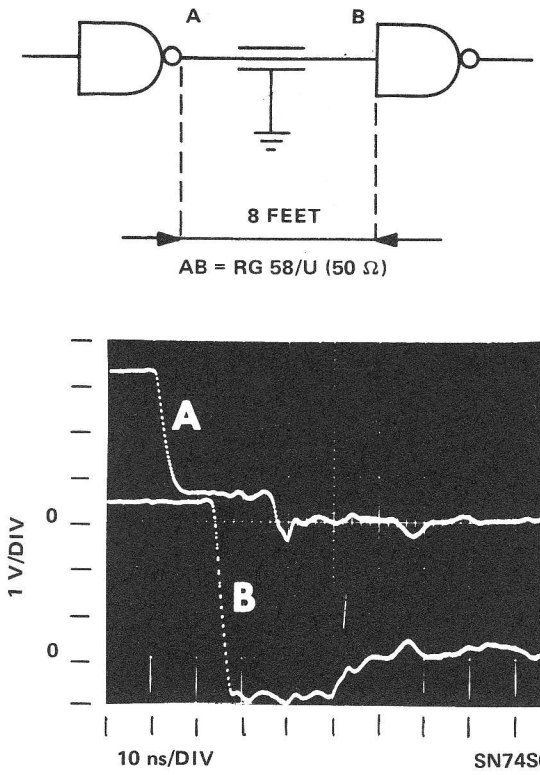


FIGURE 2.33 Negative Transition – 50-Ohm Unterminated Line

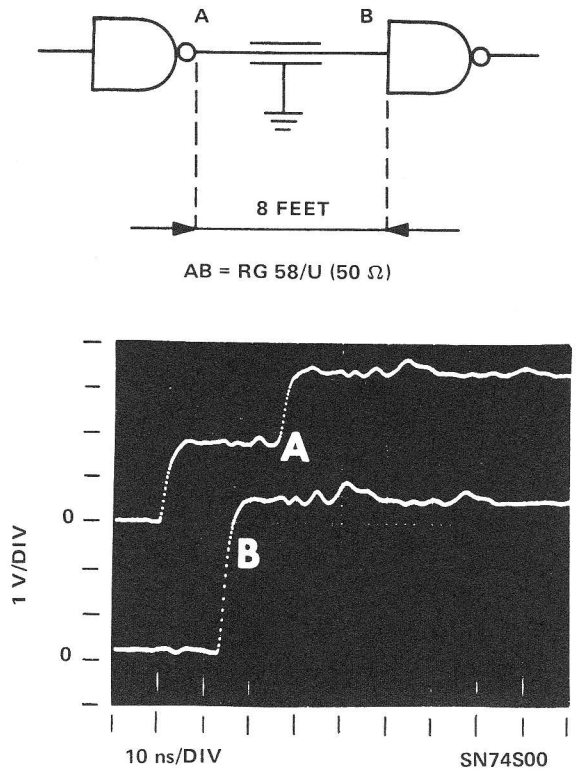


FIGURE 2.34 Positive Transition – 50-Ohm Unterminated Line

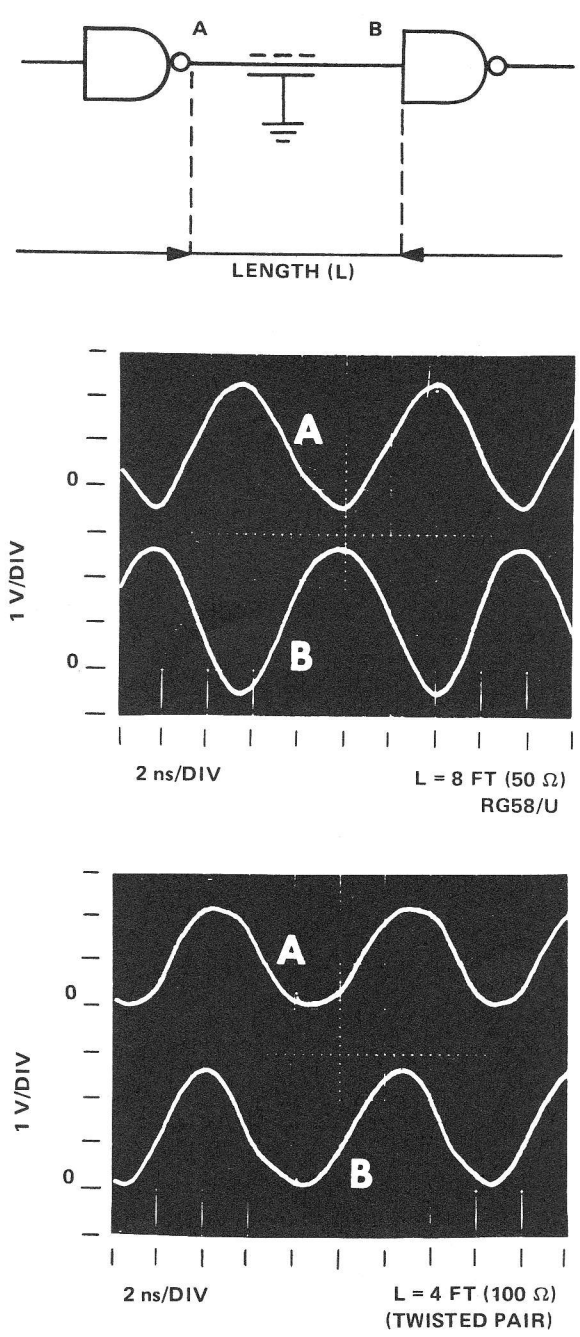


FIGURE 2.35 Unterminated Line Driving/Receiving at 125 MHz

APPENDIX A
NORMALIZED LOAD FACTORS

Normalizing output drive capability and input current requirements can prove very useful to designers of systems using two or more of the TI TTL Series of circuits. It provides a set of load factors, input current requirements in Table A-1, which can be summed and compared directly to the drive capability, Table A-2, of the output being considered. The load factor values shown are valid for any input rated at one unit load, and the output drive values are valid for any of the more common types rated for a low-logic level fan-out of 10 within its family. The more recent products added to the Series 54/74 family have been rated to drive 20 high-logic level (H) loads; therefore, the Series 54/74 capability is given both for the 10 and 20 fan-out ratings.

The loading of these type outputs can be checked from any column; however, most designs tend to utilize one of the Series as the basic building blocks, and as the tables cover each Series individually, the designer has the choice of working from the column containing the normalized fan-out familiar to him. As an example, the designers of a system using Series 74S as the basic circuits will probably find that the use of the right-hand column will suit him best, because both fan-out (Table A-2) and load factors

Table A-1. Normalized Input Current Requirements

Series	Input Level	Input Current	Input Current Normalized to					
			Series 54/74	Series 54H/74H	Series 54L/74L	Series 74LS	Series 74LS	Series 54S/74S
54/74	H	40 μA	1	0.8	4	2	2	0.8
	L	1.6 mA	1	0.8	9	4.5	4.5	0.8
54H/74H	H	50 μA	1.25	1	5	2.5	2.5	1
	L	2 mA	1.25	1	11	5.5	5.5	1
54L/74L	H	10 μA	0.25	0.2	1	0.5	0.5	0.2
	L	0.18 mA	0.11	0.09	1	0.5	0.5	0.09
54LS/74LS	H	20 μA	0.5	0.4	2	1	1	0.4
54LS	L	0.36 mA	0.225	0.18	2	1	1	0.18
74LS	L	0.36 mA	0.225	0.18	2	1	1	0.18
54S/74S	H	50 μA	1.25	1	5	2.5	2.5	1
	L	2 mA	1.25	1	11	5.5	5.5	1

Table A-2. Normalized Output Drive Capability

Series	Output Level	Output Current	Output Drive Normalized to					
			Series 54/74	Series 54H/74H	Series 54L/74L	Series 54LS	Series 74LS	Series 54S/74S
54/74	H*	400/800 μA	10/20†	8/16†	40/80†	20/40†	20/40†	8/16†
	L	16 mA	10	8	89	44	44	8
54H/74H	H*	500 μA	12.5	10	50	12.5	25	10
	L	20 mA	12.5	10	111	55	55	10
54L/74L	H*	100 μA	2.5	2	10	5	5	2
	L	2 mA	1.25	1	11	5.5	5.5	1
54LS/74LS	H*	400 μA	10	8	40	20	20	8
54LS	L	5 mA	2.5	2	22	11	11	2
74LS	L	8 mA	5	4	44	22	22	4
54S/74S	H*	1000 μA	25	20	100	50	50	20
	L	20 mA	12.5	10	111	55	55	10

*Active pull-up circuits. Open-collector drive is determined by value of pull-up resistor used.

†Second Number is Applicable for Parts Rated for I_{OH} = 800 μA.

(Table A-1) are expressed in terms compatible with the assumption that Series 74S has a low-logic-level fan-out of 10 and a high-logic level fan-out of 20. The use of these simple, easy-to-remember numbers was developed within each Series to make the verification of output loading simply a matter of counting the number of inputs connected to a particular output. When mixtures of Series are used, then a common denominator (normalized factor) becomes useful.

The verification of Series 74S output driving the loads illustrated in Figure A-1 would be another case of simply adding up all the factors and comparing that the sum does not exceed the drive capability.

Output drive capability of Series 54S/74S Schottky circuits rated to drive more than the standard 10/20 loads is summarized in Table A-3.

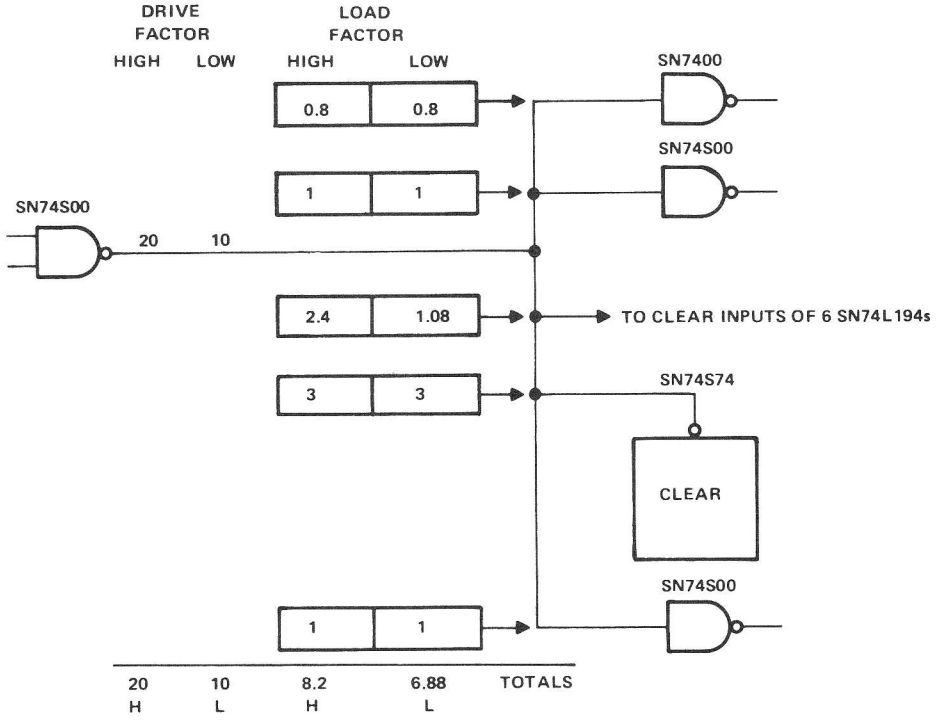


FIGURE A-1. Typical Calculation of Fan-Out

Table A-3. Fan-Out and Drive Capability for Schottky Circuits

Series	Logic-Level of Normalized Load	Standard Outputs	SN54S40 SN74S40	SN54S134	SN74S134	SN54S140 SN74S140
54/74	High	25*	75	25	12.5	50 Ω
	Low	12.5	37.5	11.8	8.7	37.5
54H/74H	High	20*	60	20	10	50 Ω
	Low	10	30	9.5	7	30
54L/74L	High	100*	300	100	50	50 Ω
	Low	111	333	105	77	333
54LS/74LS	High	50*	150	50	25	50 Ω
	Low	55	165	52	38	165
54S/74S	High	20*	60	20	10	50 Ω
	Low	10	30	9.5	7	30
Bus†Loads	HI-Z	–	–	20	120	–

*Active pull-up circuits. Open-collector drive is determined by value of pull-up resistor used.

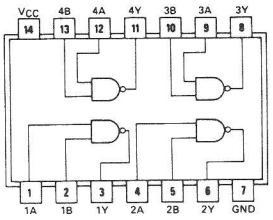
†This is the total number of these and similar three-state outputs which can be connected to a common bus and still drive the number of logic loads specified in the table.

APPENDIX B
SERIES 54S/74S PIN ASSIGNMENT DIAGRAMS
(applicable for all package types)

SN54S00
SN74S00

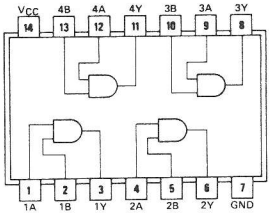
QUADRUPLE 2-INPUT
POSITIVE-NAND GATES

positive logic:
$Y = \overline{AB}$



SN54S09*
SN74S09*

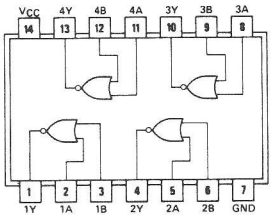
QUADRUPLE 2-INPUT
POSITIVE-AND GATES
WITH OPEN-COLLECTOR
OUTPUTS
positive logic:
$Y = AB$



SN54S02
SN74S02

QUADRUPLE 2-INPUT
POSITIVE-NOR GATES

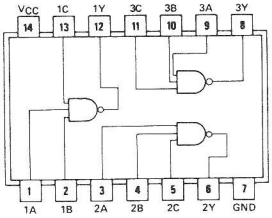
positive logic:
$Y = \overline{A + B}$



SN54S10
SN74S10

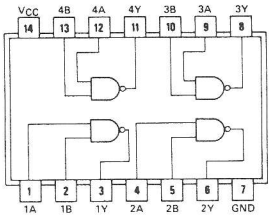
TRIPLE 3-INPUT
POSITIVE-NAND GATES

positive logic:
$Y = \overline{ABC}$



SN54S03
SN74S03

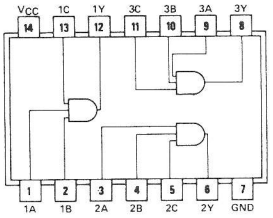
QUADRUPLE 2-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR
OUTPUTS
positive logic:
$Y = \overline{AB}$



SN54S11
SN74S11

TRIPLE 3-INPUT
POSITIVE-AND GATES

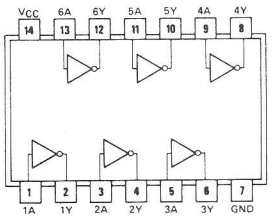
positive logic:
$Y = ABC$



SN54S04
SN74S04

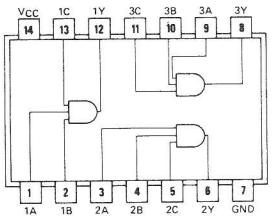
HEX INVERTERS

positive logic:
$Y = \overline{A}$



SN54S15
SN74S15

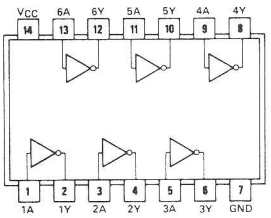
TRIPLE 3-INPUT
POSITIVE-AND GATES
WITH OPEN-COLLECTOR
OUTPUTS
positive logic:
$Y = ABC$



SN54S05
SN74S05

HEX INVERTERS
WITH OPEN-COLLECTOR
OUTPUTS

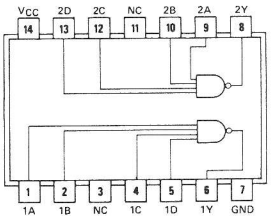
positive logic:
$Y = \overline{A}$



SN54S20
SN74S20

DUAL 4-INPUT
POSITIVE-NAND GATES

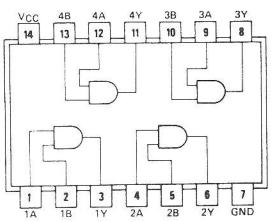
positive logic:
$Y = \overline{ABCD}$



SN54S08*
SN74S08*

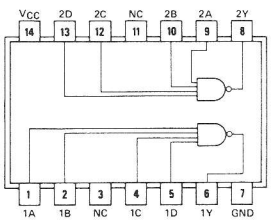
QUADRUPLE 2-INPUT
POSITIVE-AND GATES

positive logic:
$Y = AB$



SN54S22
SN74S22

DUAL 4-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR
OUTPUTS
positive logic:
$Y = \overline{ABCD}$



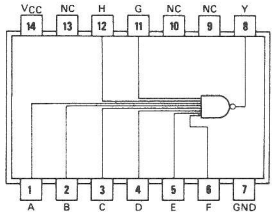
*TO BE ANNOUNCED

APPENDIX B
SERIES 54S/74S PIN ASSIGNMENT DIAGRAMS
(applicable for all package types)

SN54S30
SN74S30

8-INPUT
POSITIVE-NAND GATES

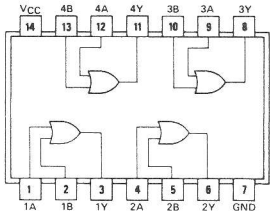
positive logic:
$Y = \overline{ABCDEFGH}$



SN54S32*
SN74S32*

QUADRUPLE 2-INPUT
POSITIVE-OR GATES

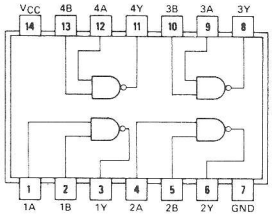
positive logic.
Y = A + B



SN54S37*
SN74S37*

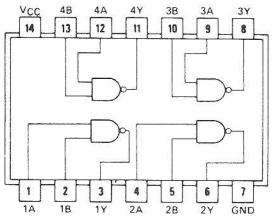
QUADRUPLE 2-INPUT
POSITIVE-NAND BUFFERS

positive logic:
$Y = \overline{AB}$



SN54S38*
SN74S38*

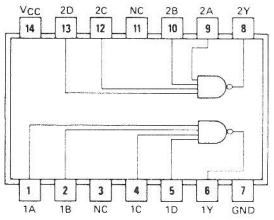
QUADRUPLE 2-INPUT
POSITIVE-NAND BUFFERS
WITH OPEN-COLLECTOR
OUTPUTS
positive logic:
$Y = \overline{AB}$



SN54S40
SN74S40

DUAL 4-INPUT
POSITIVE-NAND BUFFERS

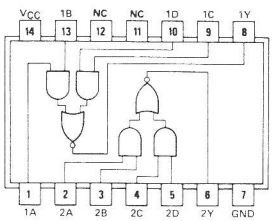
positive logic:
$Y = \overline{ABCD}$



SN54S51
SN74S51

DUAL 2-WIDE 2-INPUT
AND-OR-INVERT GATES

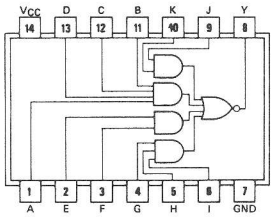
positive logic:
$Y = \overline{AB + CD}$



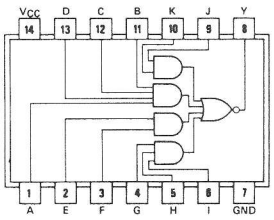
SN54S64
SN74S64

4-2-3-2-INPUT
AND-OR-INVERT GATES

positive logic:
$Y = \overline{ABCD+EF+GHI+JK}$

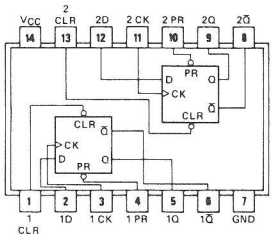


SN54S65
SN74S65
4-2-3-2-INPUT
AND-OR-INVERT GATES
WITH OPEN-COLLECTOR
OUTPUTS
positive logic:
$Y = \overline{ABCD+EF+FHI+JK}$



SN54S74
SN74S74

DUAL D-TYPE POSITIVE-
EDGE-TRIGGERED
FLIP-FLOPS

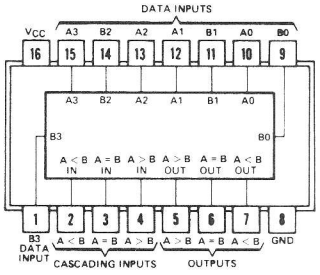


FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

SN54S85
SN74S85

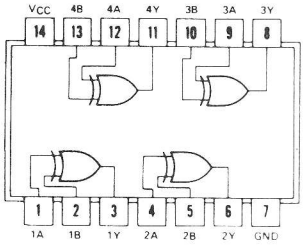
4-BIT MAGNITUDE
COMPARATORS


DATA INPUTS
VCC A3 B2 A2 A1 B1 A0 B0
16 15 14 13 12 11 10 9
A3 B2 A2 A1 B1 A0
B3 B0
A<B IN A=B IN A>B IN A>B OUT A=B OUT A<B OUT
1 2 3 4 5 6 7 8
B3 DATA INPUT
A<B A=B A>B
CASCADING INPUTS
A>B A=B A<B
OUTPUTS
GND

SN54S86
SN74S86

QUADRUPLE 2-INPUT
EXCLUSIVE-OR GATES

positive logic:
$Y = A \oplus B = \bar{A}B + A\bar{B}$

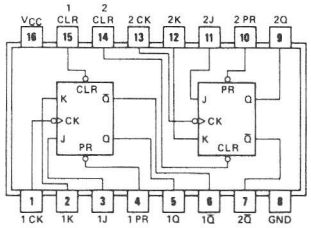


*TO BE ANNOUNCED

APPENDIX B
SERIES 54S/74S PIN ASSIGNMENT DIAGRAMS
(applicable for all package types)

SN54S112
SN74S112

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

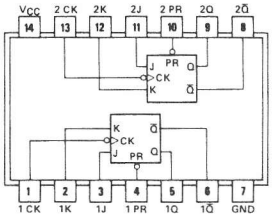


FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

SN54S113
SN74S113

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

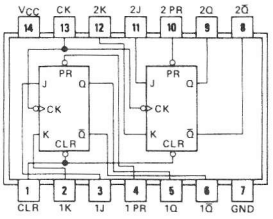


FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLOCK	J	K	Q	Q̄
L	X	X	X	H	L
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$

SN54S114
SN74S114

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK



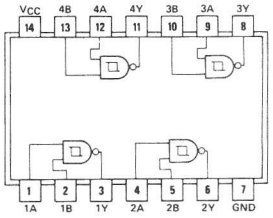
FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

SN54S132
SN74S132

QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

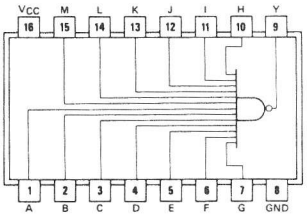
positive logic:
$Y = \overline{AB}$



SN54S133
SN74S133

13-INPUT POSITIVE-NAND GATES

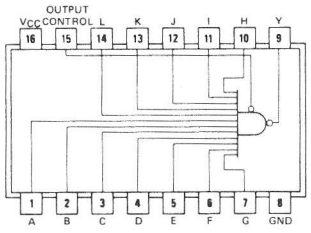
positive logic:
$Y = \overline{ABCDEFGHIJKLM}$



SN54S134
SN74S134

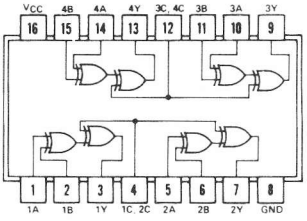
12-INPUT POSITIVE-NAND GATE WITH THREE-STATE OUTPUTS

positive logic:
$Y = \overline{ABCDEFGHIJKL}$
Output is off (disabled) when output control is high.



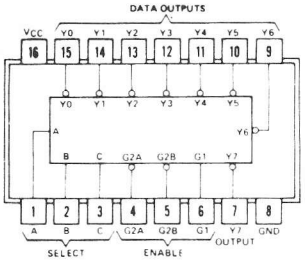
SN54S135
SN74S135

QUADRUPLE EXCLUSIVE OR/NOR GATES



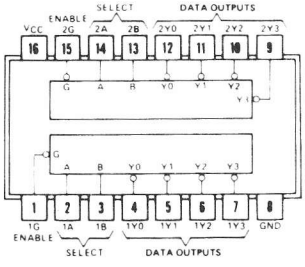
SN54S138
SN74S138

3-LINE-TO-8-LINE DECODERS/ DEMULTIPLEXERS



SN54S139
SN74S139

DUAL 2-LINE-TO-4-LINE DECODERS/ DEMULTIPLEXERS

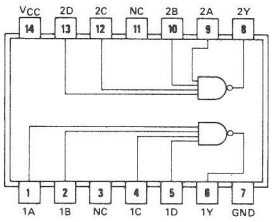


APPENDIX B
SERIES 54S/74S PIN ASSIGNMENT DIAGRAMS
(applicable for all package types)

SN54S140
SN74S140

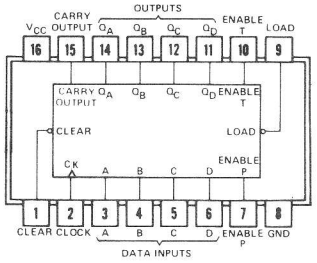
DUAL 4-INPUT
POSITIVE-NAND 50-OHM
LINE DRIVERS

positive logic:
Y = ABCD



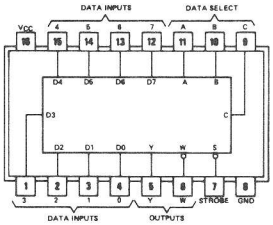
SN54S163*
SN74S163*

FULLY SYNCHRONOUS
4-BIT BINARY
COUNTERS



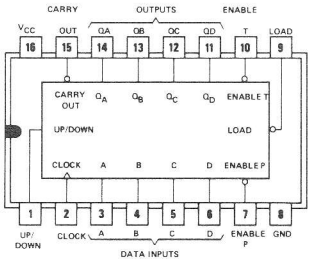
SN54S151
SN74S151

8-LINE-TO-1-LINE
DATA SELECTORS/
MULTIPLEXERS



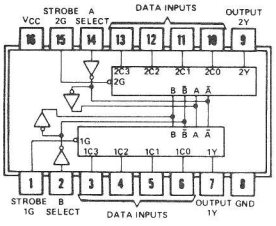
SN54S168*
SN74S168*

FULLY SYNCHRONOUS
4-BIT BCD
UP/DOWN COUNTERS



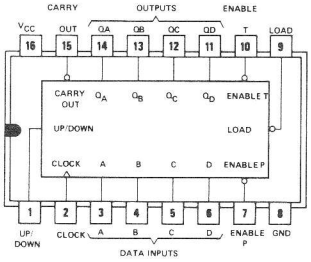
SN54S153
SN74S153

DUAL 4-LINE-TO-1-LINE
DATA SELECTORS/
MULTIPLEXERS



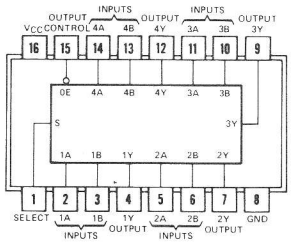
SN54S169*
SN74S169*

FULLY SYNCHRONOUS
4-BIT BINARY
UP/DOWN COUNTERS



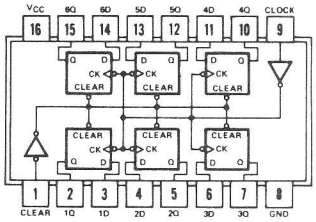
SN54S157
SN74S157

QUADRUPLE 2-LINE-TO-
1-LINE DATA SELECTORS/
MULTIPLEXERS
(NONINVERTED DATA)



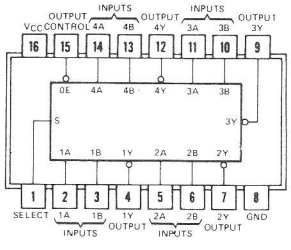
SN54S174
SN74S174

HEX D-TYPE
FLIP-FLOPS



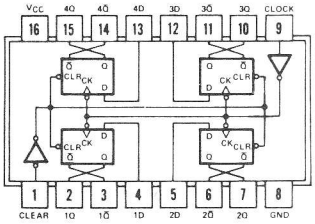
SN54S158
SN74S158

QUADRUPLE 2-LINE-TO-
1-LINE DATA SELECTORS/
MULTIPLEXERS
(INVERTED DATA)



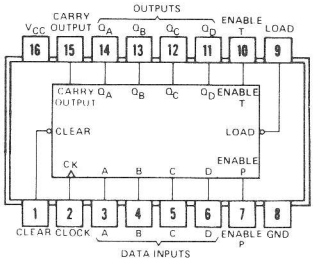
SN54S175
SN74S175

QUADRUPLE
D-TYPE FLIP-FLOPS



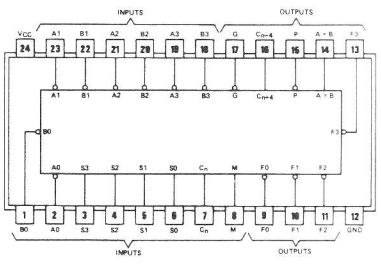
SN54S162*
SN74S162*

FULLY SYNCHRONOUS
4-BIT BCD COUNTERS



SN54S181
SN74S181

4-BIT PARALLEL
ARITHMETIC
LOGIC UNITS/
FUNCTION
GENERATORS

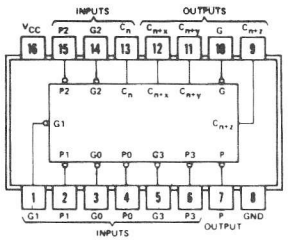

INPUTS
OUTPUTS
VCC A1 B1 A2 B2 A3 B3 G Cn+4 P A=B F3
24 23 22 21 20 19 18 17 16 15 14 13
A1 B1 A2 B2 A3 B3 G Cn+4 P A=B
B0
F3
A0 S3 S2 S1 S0 Cn M F0 F1 F2
1 2 3 4 5 6 7 8 9 10 11 12
B0 A0 S3 S2 S1 S0 Cn M F0 F1 F2 GND
INPUTS
OUTPUTS

*TO BE ANNOUNCED.

APPENDIX B
SERIES 54S/74S PIN ASSIGNMENT DIAGRAMS
(applicable for all packages)

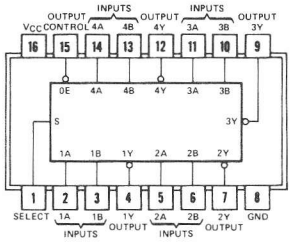
SN54S182
SN74S182

LOOK-AHEAD
CARRY GENERATORS



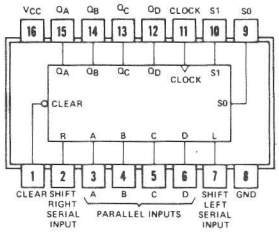
SN54S258
SN74S258

QUADRUPLE
2-LINE-TO-1-LINE
DATA SELECTORS/
MULTIPLEXERS WITH
3-STATE OUTPUTS
(INVERTED DATA)



SN54S194
SN74S194

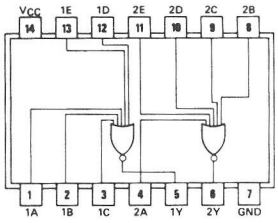
4-BIT BIDIRECTIONAL
UNIVERSAL SHIFT
REGISTERS



SN54S260
SN74S260

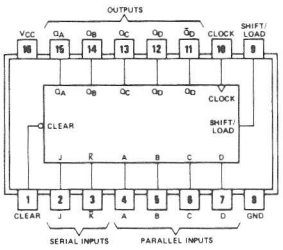
DUAL 5-INPUT
POSITIVE-NOR GATES

positive logic:
$Y = \overline{A+B+C+D+E}$



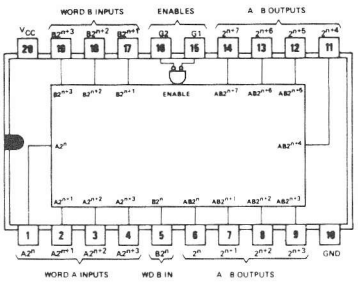
SN54S195
SN74S195

4-BIT PARALLEL-
ACCESS SHIFT
REGISTERS



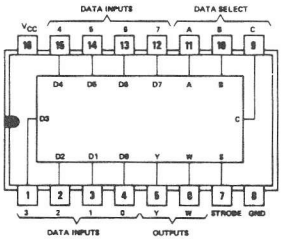
SN54S274*
SN74S274*

4-BIT-BY-4-BIT
PARALLEL
BINARY
MULTIPLIERS



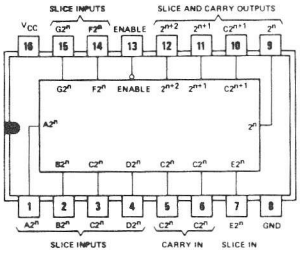
SN54S251
SN74S251

8-LINE-TO-1-LINE
DATA SELECTORS/
MULTIPLEXERS WITH
3-STATE OUTPUTS



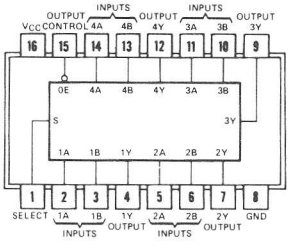
SN54S275*
SN74S275*

CASCADABLE
7-LINE BIT-SLICE
WALLACE TREES



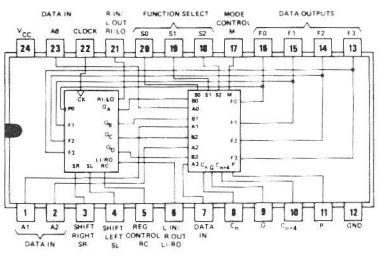
SN54S257
SN74S257

QUADRUPLE
2-LINE-TO-1-LINE
DATA SELECTORS/
MULTIPLEXERS WITH
3-STATE OUTPUTS
(NON INVERTED
DATA)



SN54S281*
SN74S281*

4-BIT PARALLEL
BINARY
ACCUMULATORS



*TO BE ANNOUNCED.

APPENDIX C

LETTER SYMBOLS, TERMS, AND DEFINITIONS

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use. The definitions are grouped into sections applying to voltages, currents, switching characteristics, and classification of circuit complexity.

VOLTAGES

V_{IH} High-level input voltage

An input voltage level within the more positive (less negative) of the two ranges of values used to represent the binary variables. A minimum value is specified which is the least-positive (most-negative) value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} Low-level input voltage

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. A maximum value is specified which is the most-positive (least-negative) value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{T+} Positive-going threshold voltage

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

V_{T-} Negative-going threshold voltage

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

V_{OH} High-level output voltage

The voltage at an output terminal for a specified output current I_{OH} with input conditions applied that according to the product specification will establish a high level at the output.

V_{OL} Low-level output voltage

The voltage at an output terminal for a specified output current I_{OL} with input conditions applied that according to the product specification will establish a low level at the output.

$V_{O(on)}$ On-state output voltage

The voltage at an output terminal for a specified output current with input conditions applied that according to the product specification will cause the output switching element to be in the on state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

$V_{O(off)}$ Off-state output voltage

The voltage at an output terminal for a specified output current with input conditions applied that according to the product specification will cause the output switching element to be in the off state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

CURRENT

I_{IH} High-level input current

The current flowing into* an input when a specified high-level voltage is applied to that input.

I_{IL} Low-level input current

The current flowing into* an input when a specified low-level voltage is applied to that input.

I_{OH} High-level output current

The current flowing into* the output with a specified high-level output voltage V_{OH} applied.

Note: This parameter is usually specified for open-collector outputs intended to drive other logic circuits.

*Current flowing out of a terminal is a negative value.

CURRENTS (continued)

$I_{O(off)}$ Off-state output current

The current flowing into* an output with a specified output voltage applied and input conditions applied that according to the product specification will cause the output switching element to be in the off state.

Note: This parameter is usually specified for open-collector outputs intended to drive devices other than logic circuits or for three-state outputs.

I_{OS} Short-circuit output current

The current flowing into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{CCH} Supply current, output(s) high

The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a high-level voltage.

I_{CCL} Supply current, output(s) low

The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a low-level voltage.

DYNAMIC CHARACTERISTICS

f_{max} Maximum clock frequency

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause a change of output state with each clock pulse.

t_{HZ} Output disable time (of a three-state output) from high level

The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{LZ} Output disable time (of a three-state output) from low level

The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PLH} Propagation delay time, low-to-high-level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PHL} Propagation delay time, high-to-low-level output

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{TLH} Transition time, low-to-high-level output

The time between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level.

t_{THL} Transition time, high-to-low-level output

The time between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level.

t_w Average pulse width

The time between 50-percent-amplitude points (or other specified reference points) on the leading and trailing edges of a pulse.

t_{hold} Hold time

The time interval for which a signal or pulse is retained at a specified input terminal after an active transition occurs at another specified input terminal.

*Current flowing out of a terminal is a negative value.

DYNAMIC CHARACTERISTICS (continued)

$t_{release}$ Release time

The time interval between the release from a specified input terminal of data intended to be recognized and the occurrence of an active transition at another specified input terminal.

Note: When specified, the interval designated "release time" falls within the setup interval and constitutes, in effect, a negative hold time.

t_{setup} Setup time

The time interval for which a signal is applied and maintained at a specified input terminal before an active transition occurs at another specified input terminal.

t_{ZH} Output enable time (of a three-state output) to high level

The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{ZL} Output enable time (of a three-state output) to low level

The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

CLASSIFICATION OF CIRCUIT COMPLEXITY

Gate equivalent circuit

A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

LSI Large-scale integration

A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether logical or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

MSI Medium-scale integration

A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

SSI Small-scale integration

Integrated circuits of less complexity than medium-scale integration (MSI).

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4. R. S. Singleton, "No Need to Juggle Equations to Find Reflections – Just Draw Three Lines," *Electronics*, October 28, 1968.
5. *Designing with TTL Integrated Circuits* (McGraw-Hill Book Co., New York), pp. 25-45 and pp. 83-105, 1971.

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Printed in U.S.A. 09-73-60083-15M